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METRIC

VANGUARD I (10 MB)
REMOVABLE CARTRIDGE DISK SYSTEM
INSTALLATION AND MAINTENANCE MANUAL

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PREFACE

This manual provides the required information to install and configure the Perkin-Elmer Vanguard I (10 Mb) Removable Cartridge Disk System.

Chapter 1 contains a general description of the system. Chapter 2 describes the installation of the system, including configuration specifications. Power requirements are also contained in this chapter. Chapter 3 discusses the operation, programming instructions, and a detailed schematic analysis of each major section in the system. A mnemonics list is located at the end of the chapter.

The readership level of this manual is geared to the people who require information to install and perform maintenance on the system assemblies. The following publications provide additional information on the Perkin-Elmer Vanguard I (10 Mb) Removable Cartridge Disk System:

Common 2.5 and 10 Megabyte Disk Test Program, Publication Number 06-173

Common 2.5 and 10 Megabyte Disk Formatter Test Program, Publication Number 06-251

Vanguard I Vendor Operation and Maintenance Manual, Vol. I Publication Number 29-738

Vanguard I Vendor Operation and Maintenance Manual, Vol. II, Publication Number 29-739

2.5 and 10 Megabyte Removable Cartridge Disk Programming Manual, Publication Number 29-454

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DRAWINGS

Information Drawing, Installation and Voltage Conversion, Vanguard I	02-708R00C12
Functional Schematic Drawing, Disk Controller	02-263R06D08
Assembly Drawing, Cartridge Disk Controller	35-438M01R12E03

CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The Perkin-Elmer Vanguard I (10 Mb) Removable Cartridge Disk System consists of a single 381 mm (15") controller, interconnecting cables, and from one to four disk drives.

Table 1-1 describes the relationship between hardware-related product numbers and part numbers for different configurations of the removable cartridge disk system.

TABLE 1-1 REMOVABLE CARTRIDGE DISK SYSTEM CONFIGURATIONS

1600

MARKETING NUMBER	PART NUMBER	QUANTITY	CONTENTS	DESCRIPTION
M46-710		1	35-438F01M01	Controller
115 V	02-708F01	1	17-278	Main cable
System		1	27-121F01	10 Mb disk (115 V, ±10%, 47-63 Hz)
		1	27-056	Cartridge
M46-712		1	27-121F01	10 Mb disk (115 V, ±10%, 47-63 Hz)
115 V	02-709F01			
Expansion		1	17-279	Expansion cable
		1	27-056	Cartridge
M46-711		1	35-438F01M01	Controller
230 V	02-708F02	1	17-278	Main cable
System		1	27-121F02	10 Mb disk (230 V, ±10%, 47-63 Hz)
		1	27-056	Cartridge
M46-713		1	27-121F02	10 Mb disk (230 V, ±10%, 47-63 Hz)
230 V	02-709F02			
Expansion		1	17-279	Expansion cable
		1	27-056	Cartridge

CHAPTER 2
INSTALLATION

2.1 MECHANICAL ASSEMBLY

The Perkin-Elmer Vanguard I (10 Mb) Removable Cartridge Disk System consists of a single 381 mm (15") printed circuit controller (35-438F01M01), interconnecting cables (17-278 or 17-279), and one to four disk drives. Mounting and voltage conversion instructions of the disk drive are shown in Information Drawing 02-708C12, which is provided in this manual.

2.2 AC POWER REQUIREMENTS

All removable cartridge disk drives are normally equipped for 115 V ±10%, 47-63 Hz operation. A jumper plug change is required in the disk power supply, which is internal to the disk drive itself for operation with 230 V ±10%, 47-63 Hz. (Refer to Information Drawing 02-708C12.) Start-up current is 3.5 A for 24 seconds with a drop to 2.5 A when disk speed is attained.

2.3 UNPACKING INSTRUCTIONS

There are no special unpacking instructions for the Perkin-Elmer Vanguard I (10 Mb) Removable Cartridge Disk System; however, caution should be taken when handling the disk drive after it has been uncrated.

2.4 MOUNTING INSTRUCTIONS

The removable cartridge disk drive can be mounted in any standard 483 mm (19") Retma cabinet or rack. All necessary hardware is included for mounting the drive in a Perkin-Elmer rack. For mounting instructions and procedures, refer to Information Drawing 02-708C12 in this manual, and to Vendor Maintenance Manual, Publication Number 29-738.

2.5 SYSTEM CONFIGURATION

The removable cartridge disk controller may be installed in any standard 381 mm (15") I/O slot of a Perkin-Elmer processor or expansion card file. Remove the RACK0/TACK0 strap between backpanel terminals 122-1 and 222-1 at the controller location. The controller device addresses are normally wired for X'B6', X'C6', C'D6', X'E6', and X'F6'. The address strapping at the controller must be altered if other than the normal set is desired.

2.5.1 1x1 Removable Cartridge Disk System Configuration

Figure 2-1 shows the configuration and interconnecting cable connections for a 1x1 removable cartridge disk system.

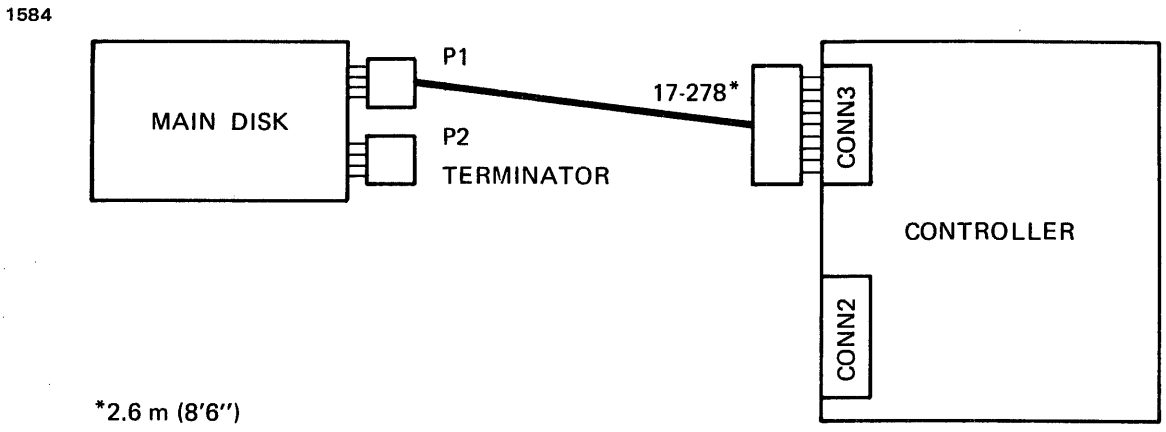

Figure 2-1 1x1 Removable Cartridge Disk System Configuration

2.5.2 1x2 Removable Cartridge Disk System Configuration

Figures 2-2 and 2-3 show the configuration and interconnecting cable connections for a 1x2 removable cartridge disk system. The terminator must be moved to the last disk drive.

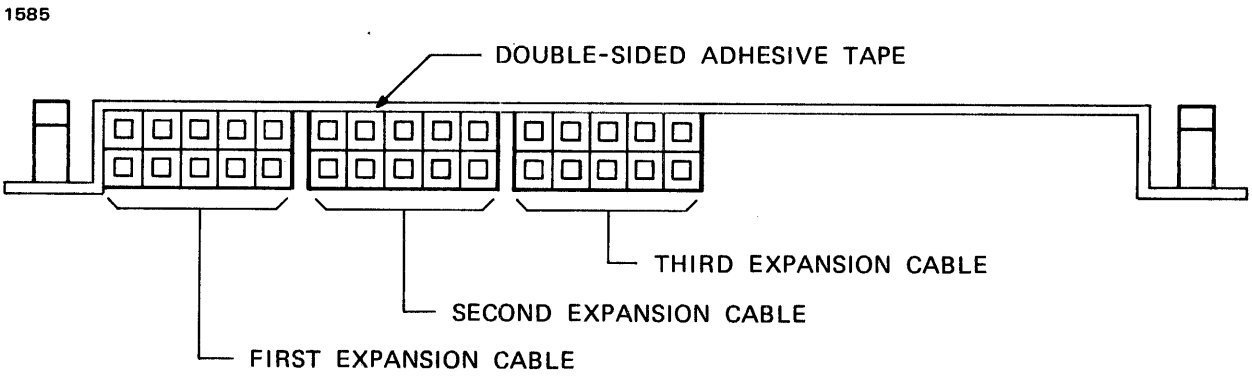

Figure 2-2 Expansion Cable Connections

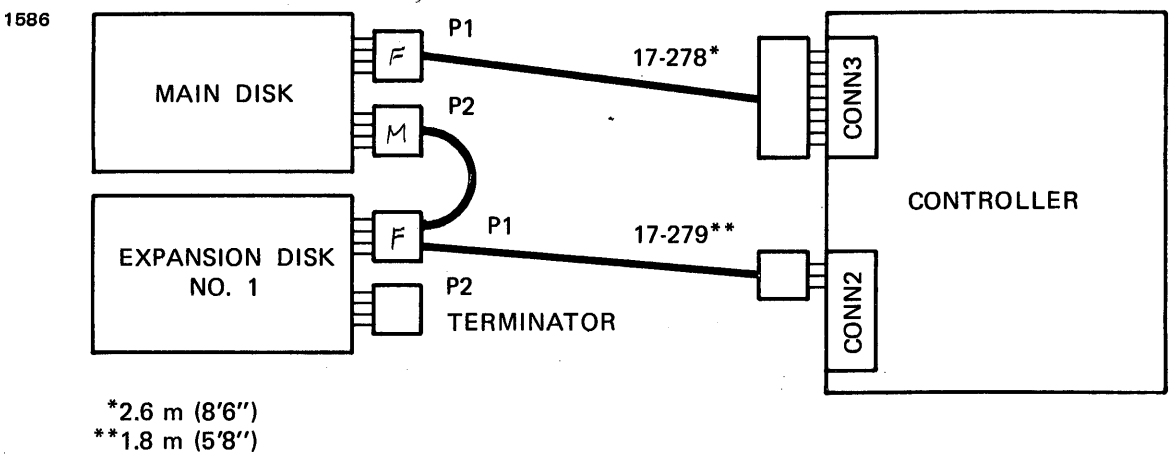

Figure 2-3 1x2 Removable Cartridge Disk System Configuration

2.5.3 1x3 Removable Cartridge Disk System Configuration

Figures 2-2 and 2-4 show the configuration and interconnecting cable connections for a 1x3 removable cartridge disk system. The terminators must be removed from the first and second disk drives.

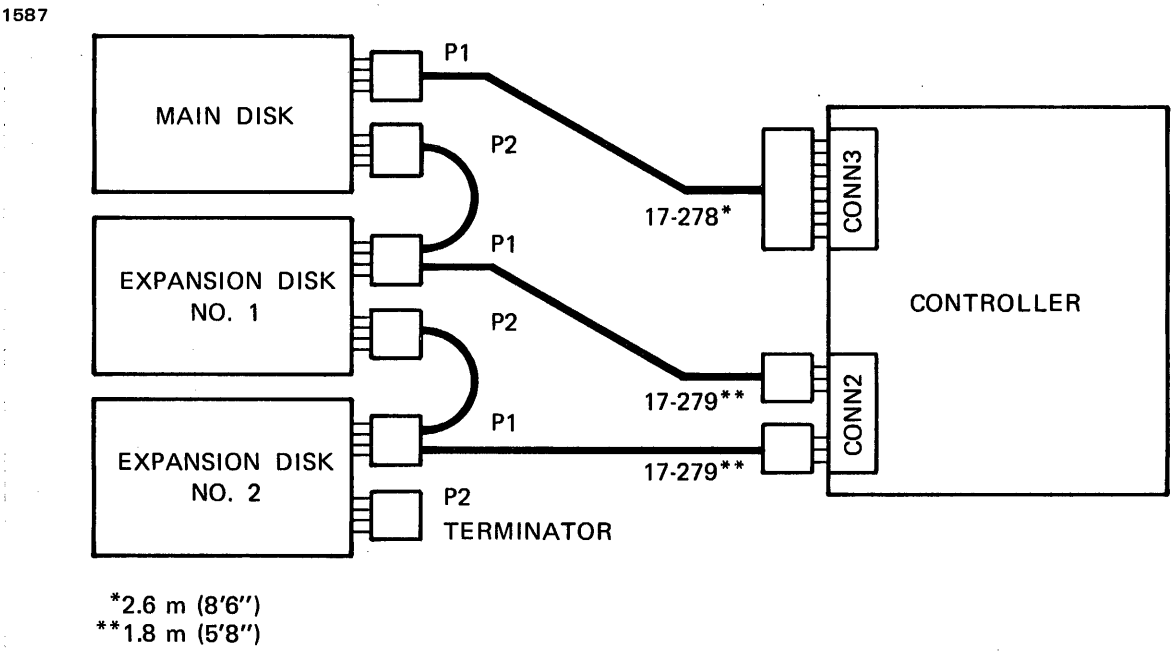

Figure 2-4 1x3 Removable Cartridge Disk System Configuration

2.5.4 1x4 Removable Cartridge Disk System Configuration

Figure 2-5 shows the configuration and interconnecting cable connections for a 1x4 removable cartridge disk system. The terminators must be removed from the first, second, and third disk drives.

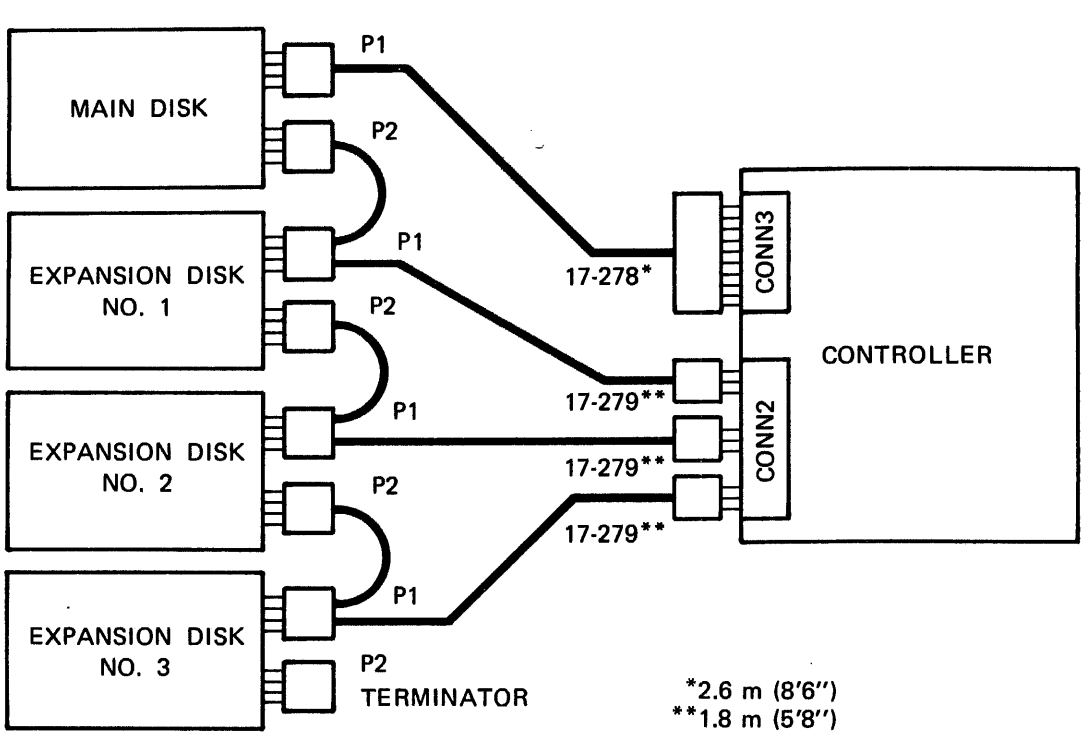

Figure 2-5 1x4 Removable Cartridge Disk System Configuration

2.6 CABLES

There are two different cables for the system. The cables required are determined by the number of disk drives per system. (Refer to Table 2-1.)

TABLE 2-1 CABLES

DISK DRIVES PER SYSTEM	CABLES PER SYSTEM	PART NUMBER
1	1	17-278
2	1 1	17-278 17-279
3	1 2	17-278 17-279
4	1 3	17-278 17-279

2.7 TESTING

Load Test Program 06-173 and run the tests as described in Test Program Description 06-173A15.

2.8 DEVICE ADDRESS STRAPPING

The preferred addresses for the removable cartridge disk controller are X'B6', X'C6', X'D6', X'E6', and X'F6'. Wirewrap stakes are available on the controller for address strapping. Refer to Functional Schematic 02-263D08 for details.

2.9 ADJUSTMENTS

There are five adjustments required on the controller. They are:

1. read delay
2. write delay
3. guard delay
4. write switching delay
5. sector mark

Adjustment procedures are:

1. Load Test Program 06-173 and run Test 8 (Spiral Data Test). Set the LOOP option to FFFF and turn off the Teletype while Test 8 is running.

2. Adjust potentiometer R59, associated with the sector mark, for a time period of 5±1 microseconds (pin 5 of A56).

3. Adjust potentiometer R61, associated with the read delay, for a time period of 65±4 microseconds (pin 6 of A97).

4. Adjust potentiometer R63, associated with the write delay, for a time period of 36±2 microseconds (pin 6 of A95).

5. Adjust potentiometer R79, associated with the guard delay, for a time period of 5±1 microseconds (pin 13 of A139).

6. Adjust potentiometer R66, associated with the write switching delay, for a time period of 6±1 microseconds (pin 5 of A107).

Counterclockwise rotation of the shaft decreases the resistance of these potentiometers.

2.10 MAINTENANCE

No maintenance is required on the controller; however, there is preventive maintenance required on the disk drive. Refer to the Vendor Maintenance Manual, Publication Number 29-738, for maintenance procedures.

CHAPTER 3
OPERATION

3.1 INTRODUCTION

The controller, which is used on the SELCH bus, handles all communication between the processor and the disk drives. Each controller can support from one to four disk drives with overlapping Seek and Data Transfer.

3.2 SCOPE

This chapter provides the information necessary to maintain the Perkin-Elmer Vanguard I (10 Mb) Removable Cartridge Disk Controller. Included in this chapter are a simplified block diagram, device address strapping, timing information, functional schematic analysis, and a mnemonics list.

3.3 SYSTEM BLOCK DIAGRAM

A simplified block diagram of the system is shown in Figure 3-1.

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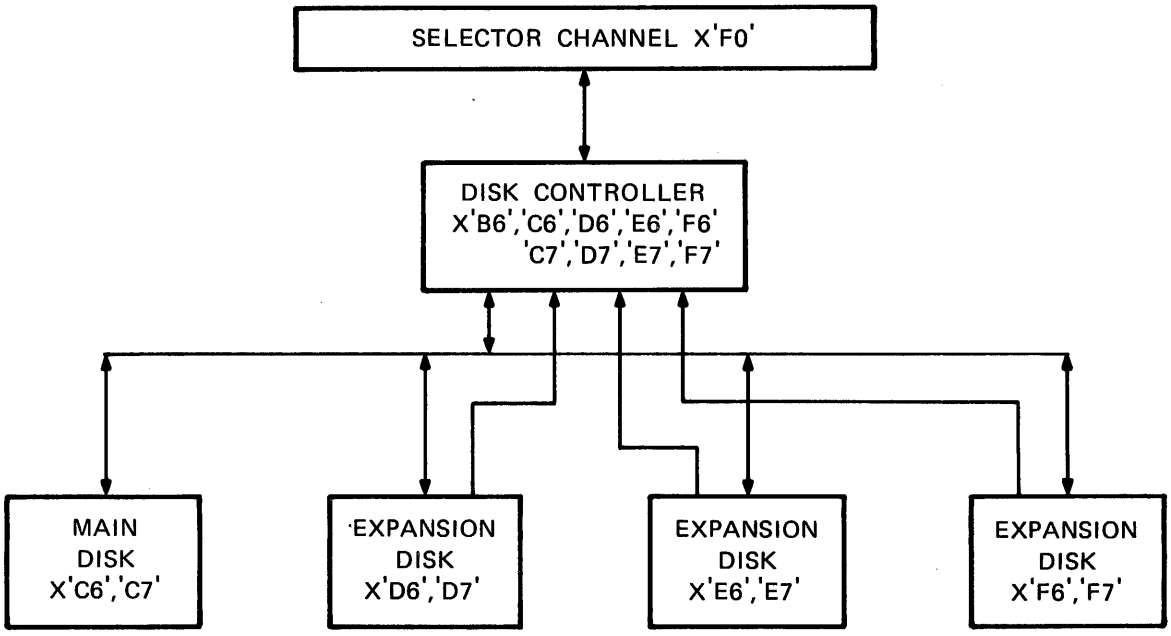


Figure 3-1 Simplified Block Diagram

3.4 PROGRAMMING INSTRUCTIONS

Table 3-1 summarizes the controller status byte.

TABLE 3-1 CONTROLLER COMMAND, STATUS, AND DATA BYTES

INST BIT	0	1	2	3	4	5	6	7	
CMD	X	X	X	X	0	0	0	1	READ
	X	X	X	X	0	0	1	0	WRITE
	X	X	X	X	0	0	1	1	READ CHECK
	X	X	X	X	0	1	0	1	READ FORMAT
	X	X	X	X	0	1	1	0	WRITE FORMAT
	X	X	X	X	1	X	X	X	RESET
WD	0	0	HEAD 0/1	SECT 16	SECT 8	SECT 4	SECT 2	SECT 1	
WD	CYL 128	CYL 64	CYL 32	CYL 16	CYL 8	CYL 4	CYL 2	CYL 1	
RD (CONTROLLER IDLE)	0	0	0	SECT 16	SECT 8	SECT 4	SECT 2	SECT 1	
SS	OVER-RUN	ADDR COMP FAIL	DEF TRK	CYL OV	BSY	EX	CONT IDLE	DATA TRANSFER ERROR	

X = Don't care

3.4.1 Controller Command Definitions

The controller contains interrupt circuits which are always enabled; therefore, the standard Enable/Disable command bits are not used.

READ — Enables the controller to perform a normal data read. The Selector Channel must be set up prior to the command, the heads must be positioned, and the sector address must be loaded in the controller. The data transfer from the controller delays for at least 90 microseconds after a sector match. The Selector Channel must be started before this time. If the last sector read is not a complete sector, the Selector Channel terminates after the last byte is read into core, but the controller continues reading until the longitudinal parity error check word is verified, and then sets CONT IDLE.

WRITE — Enables the controller to perform a normal data write. The Selector Channel must be set up prior to the command, the heads must be positioned, and the sector address must be loaded into the controller. Data transfer to the controller is delayed for at least 90 microseconds after a sector match. The Selector Channel must be started before this time. If the last sector written is not a complete sector, the Selector Channel terminates after the last data byte is written. The controller, however, continues and fills the remainder of the sector with the last data byte, writes the longitudinal parity error check word, and then sets CONT IDLE.

READ CHECK — Causes the controller to perform an off-line read of a single sector. The Selector Channel is not used, but the heads must be positioned and the sector address must be loaded before this command is issued. While in the READ CHECK mode, no data is passed to the Selector Channel, but the disk interface cannot be used until this mode is terminated (Controller Idle=1). The OVERRUN, ADDR COMP FAIL, DEF TRK, CONT IDLE, and LONGITUDINAL PARITY ERROR status bits have the same meaning as in the normal read. An interrupt is generated when the READ CHECK is completed (CONT IDLE $\longrightarrow$ 1). The Selector Channel can be used following the issue of the READ CHECK command.

WRITE FORMAT — This command, together with the FORMAT switch in the controller ON position, permits writing into the header field of the sector. This is normally used only when performing a surface analysis of a new cartridge. Normally, 270_{10} bytes are written in the FORMAT mode. This includes the sync field, header field, gap, data field, and longitudinal parity error check word field, in that order.

READ FORMAT — This command, together with the FORMAT switch in the controller ON position, permits reading from the header field of the sector. This is normally used only when performing a surface analysis of a new cartridge.

RESET — This command disarms all the files, resets the Attention flip-flop, Mode flip-flop, Head Select flip-flop, Data Input Register, OVERRUN, ADDR COMP FAIL, DEF TRK, CYL OV, LONGITUDINAL PARITY ERROR and WPV, and sets CONT IDLE and controller BUSY. In addition, it terminates any data transfers in progress and inhibits writing. This command does not affect a SEEK in progress and is normally required to reset status bits.

NOTE

If a nonvalid command is issued to the controller, or a format command is issued when the controller format switch is in the nonformat mode, the controller status becomes busy until a reset command or a system clear is received.

3.4.2 Controller Read Data Definition

This read data must be issued when CONT IDLE=1 and causes the sector byte of the previously selected disk to be returned to the processor. This sector byte may be changing at the time of the RD. For this reason, it is necessary to issue consecutive RDs and verify that the bytes are the same; if not, another RD must be issued.

3.4.3 Controller Write Data Definition

This byte represents the starting sector and head address for a data transfer and must be loaded before every data transfer. Only sector addresses between zero and 23_{10} are valid. Any out-of-range sector address results in an OVERRUN status.

3.4.4 Controller Status Definitions

Table 3-1 summarizes the controller status byte.

OVERRUN — This status bit is active if the sector address (set up by the WD) does not compare with any sector address from the selected disk. This bit is active after two revolutions of the disk when a sector match is not found and sets EX to generate a SELCH interrupt. When OVERRUN $\longrightarrow$ 1, CONT IDLE is set to 1. OVERRUN is reset by INITIALIZE or a command to the controller. OVERRUN occurs as a result of the program selecting a sector address $> 23_{10}$ or for certain hardware malfunctions.

ADDRESS COMPARE FAILURE	This status bit is set only in the NORMAL READ, NORMAL WRITE, or READ CHECK modes if the cylinder address, head, and sector bytes from the processor do not agree with the cylinder address, head, and sector read from the header. (Refer to Figure 3-1.) The cylinder address and sector are tested only on the first sector of a record. The head bit, however, is tested on each sector of a record. ADDRESS COMPARE FAILURE causes the READ/WRITE/READ CHECK to abort (no further data transfers occur). EX is set and an interrupt is generated when this bit gets set. This bit is reset by INITIALIZE or a command to the controller.
DEF TRK	This status bit is set only in the NORMAL READ, NORMAL WRITE, or READ CHECK modes when a data transfer is attempted on a sector which is flagged as defective (DEF TRK bit in the header field is set). The data transfer is aborted and DEF TRK sets EX and generates a SELCH interrupt. This bit is reset by INITIALIZE or by a command to the controller. This bit is tested on each sector of a record.
CYL OV	Cylinder Overflow is set when a data transfer is attempted across a cylinder boundary (head 1, sector 23). CYL OV is reset by INITIALIZE or a command to the controller. In the latter case, CYL OV is reset while CONT IDLE is being set.
BSY	This status bit is used only by the SELCH and should be ignored by programmers.
EX	EXAMINE is active while any of the following bits are set: OVERRUN, ADDR COMP FAIL, DEF TRK, or CYL OV. EX, when set, causes a SELCH interrupt.
CONTROLLER IDLE	This bit is zero when a command is sent to the controller or when a SEEK or RESTORE command is being initiated on a disk. It is set when the operation is complete, or by INITIALIZE, COMMAND RESET, or OVERRUN. In the case of SEEK or RESTORE, it is reset for approximately 40 microseconds after receipt of the command.
DATA TRANSFER ERROR	This status indicates that an error has occurred during data transfer.

LONGITUDINAL PARITY ERROR

If the controller is in the READ, READ FORMAT, or READ CHECK mode, and if a longitudinal parity error occurs, this bit is set. For multisector read operations, this bit may be set at the end of any sector. In the case of a partial sector read operation, the SELCH interrupts after the last byte is read from the disk, but the controller continues reading until the end of sector and sets CONT IDLE. If this sector has a longitudinal parity error, this status bit is set before CONT IDLE→1. This status bit is reset by INITIALIZE or a command to the controller.

WRITE PROTECT VIOLATION (WPV)

This bit is set when a write protected disk is addressed and the controller is commanded to the WRITE or WRITE FORMAT mode. This bit, when set, causes a SELCH interrupt. This status bit can be reset only by manually removing the WRITE PROTECT condition or by issuing a command to the controller which does not specify WRITE or WRITE FORMAT. WRITE PROTECT is optional on each physical disk. If this option is not provided, the WPV status is forced to zero. Any read operation is performed normally on a write protected disk. Note that each disk has a separate status byte which includes a bit to indicate that the disk is or is not write protected.

DEVICE UNAVAILABLE (DU)

If set (DU=1), this bit indicates any of the following conditions:

- the selected disk drive is not supplied with proper power or is not loaded with a disk cartridge,
- the LOAD/RUN switch is in the LOAD position,
- the disk start-up cycle is not complete,
- the write check flip-flop is set.

The bit is reset (DU=0) when none of the above conditions are true.

WRITE CHECK — If set (WRITE CHECK→1), this condition indicates that during a write operation the Write Check flip-flop is set or the supplied voltage to the disk drive has dropped to less than a nominal voltage. If this occurs, it may be desirable to rewrite the affected record. It is reset by INITIALIZE or a command to the controller.

DATA OVERFLOW — This is set to indicate that the buffer register is loaded from the disk before the previous data has been transferred to the SELCH, or that the same data is transferred twice to the disk before the next data has been sent out from the SELCH. It is reset by INITIALIZE or a command to the controller.

NOTE

When system power is turned on, the controller may select any disk. If a nonexistent disk is selected, the Device Unavailable status bit cancels out any operation. Therefore, before sensing the controller status bits for the first time after power failure, an output command to the existent disk should be issued. For example: issue an OC DISARM.

3.4.5 Disk Command, Status, and Data Bytes

Table 3-2 summarizes the disk command, status, and data bytes.

TABLE 3-2 DISK COMMAND, STATUS, AND DATA BYTES

BITS INST.	0	1	2	3	4	5	6	7	
CMD	DIS	EN	X	X	X	X	SEEK	RESTORE	
WD								256	CYLINDER ADDRESS*
WD	128	64	32	16	8	4	2	1	BYTE
SS	WRT PROT	WRT CHK	ILL ADDR	DISK ADDR INTLK	RSRW	EX	SEEK INC	DISK READY	

The command, status, and data bytes in Table 3-2 are valid for each disk. If a command is directed to an unequipped disk, the hardware responds as if the disk was equipped; i.e., a false sync does not result. If the command specifies SEEK or RESTORE, the controller locks up, waiting for control signals from a nonexistent disk. In this case, it is necessary to issue a controller command RESET.

If a Write Data is directed to an unequipped disk, the hardware responds as if the disk was equipped.

If a Sense Status is directed to an unequipped disk, the returned status byte is X'09'.

3.4.6 Disk Command Definitions

DISABLE/ENABLE

These bits control the Enable/Disable/Disarm functions as follows:

BIT NUMBER	0	1	
	1	1	DISARM - Interrupts are not queued.
	1	0	DISABLE - Interrupts are queued, but not passed to the processor.
	0	1	ENABLE - Interrupts are passed to the processor as they occur.
	0	0	NO CHANGE

SEEK

This command is used to reposition the heads to a different cylinder. The user must issue a WD CYL ADDR prior to issuing a SEEK command. The status bits SEEK INC, $\overline{\text{RSRW}}$, and DISK ADDR INTLK must be inactive (0) before issuing a SEEK. The success or failure of a SEEK is reflected in the $\overline{\text{RSRW}}$ and SEEK INC status bits. When attempting consecutive SEEK to more than one drive, the user must sense status of CONT IDLE and wait for CONT IDLE⟶1 (no interrupt is generated in this case).

After a SEEK is issued to the first disk, it takes approximately 40 microseconds for CONT IDLE⟶1.

RESTORE — This command causes the heads to move to cylinder 000. A RESTORE command is required to clear the SEEK INC status. The RSRW bit need not be zero before issuing this command, but while a RESTORE is in progress, $\overline{\text{RSRW}}$ is active. DISK ADDR INTLK must be zero before issuing a RESTORE. Worst case RESTORE time is 1.75 seconds.

3.4.7 Disk Write Data Definition

This write data is used to load the cylinder address prior to a SEEK or RESTORE. A cylinder address of 000 to 202_{10} is valid. Cylinder 000 is at the outer periphery of the disk and 202_{10} is at the inner periphery. An out-of-range cylinder address results in ILL ADDR when a SEEK or RESTORE is attempted.

3.4.8 Disk Status Definitions

The following definitions are valid only when CONT IDLE=1:

WRT PROT — If the Write Protect option is equipped and activated (as indicated by the PROTECT lamp on the disk being on), the WRT PROT status bit is active. This status bit should be tested before attempting a WRITE or WRITE FORMAT operation. (Refer to WRITE PROTECT manual controls.)

WRT CHK — This status bit is active if the disk hardware detects a fault which affects reliable WRITE operations. This fault can be improper hardware head selection or DC voltages out of specification. A permanent fault latches WRT CHK and also activates DISK NOT READY to generate an interrupt. A voltage fluctuation can cause this bit to become momentarily active. If this bit is permanently active, the disk must be shut down to determine the fault. No software recovery is possible.

ILL ADDR — This status bit is active when a SEEK or RESTORE is attempted to an out-of-range cylinder address. SEEK does not occur if attempted to an out-of-range address. If a RESTORE is attempted to an out-of-range address, the operation continues normally. ILL ADDR is reset only by a legal (in-range) SEEK or a RESTORE.

DISK ADDR INTLK — This bit is active when CONT IDLE is inactive or when the disk is in the WRITE/WRITE FORMAT mode and is in the process of writing or tunnel erase. It is active for approximately 160 microseconds after CONT IDLE⟶1 at the termination of a WRITE/WRITE FORMAT. At the end of the above operation, the user must verify that DISK ADDR INTLK⟶0 before addressing any other disk. The bit also sets EX and allows the user to sense CONT IDLE status.

3.5 FUNCTIONAL SCHEMATIC ANALYSIS

3.5.1 Introduction

The Perkin-Elmer Disk Controller is designed to connect one to four disk drives to a Perkin-Elmer computer equipped with a Selector Channel.

Refer to the timing diagrams, Figures 3-2 through 3-9, during this discussion.

The location shown for a signal or device may refer to the location on the PC board or to the location on the drawings. In this manual, references are primarily to schematics. Occasionally, when further detail is necessary, the board pin number is also given. A reference such as 2A6 refers to Functional Schematic 02-263D08, Sheet 2, coordinate block A6. A particular pin is referred to as A19-8, shown at 2A6. Refer to Sheet 2 of the schematic at grid square A6 and locate pin 8 of logic element A19.

3.5.2 Computer Interface and File Control Section

3.5.2.1 Controller Addresses

Each disk file has a unique address, and the controller has its address. These addresses must be consecutive. Of the eight address bits, five bits (0, 4, 5, 6, and 7) must be identical for the files. For example:

Data Lines	Bits 0	123	4567	
X'B6'	1	011	0110	Data Controller
X'C6'	1	100	0110	Disk File 0, Removable Disk
X'D6'	1	101	0110	Disk File 1, Removable Disk
X'E6'	1	110	0110	Disk File 2, Removable Disk
X'F6'	1	111	0110	Disk File 3, Removable Disk
X'C7'	1	100	0111	Disk File 0, Fixed Disk
X'D7'	1	101	0111	Disk File 1, Fixed Disk
X'E7'	1	110	0111	Disk File 2, Fixed Disk
X'F7'	1	111	0111	Disk File 3, Fixed Disk

The three remaining bits must be as follows:

Bit 123	
011	Data Controller
100	Disk File 0
101	Disk File 1
110	Disk File 2
111	Disk File 3

Controller addressing logic is shown on Sheet 2 of the schematic.

The data lines from the computer enter at 2G1 to 2M1 and go to the address straps. The three data lines which distinguish between the five addresses of this controller are not strapped.

The ADRS0 signal from the computer enters at Sheet 2F1. If the controller or the file is addressed, CNTAD or FLAD (2M8) is set at the trailing edge of ADRS1; otherwise, both are reset. If the controller or the file is addressed, the decoded address gates ADRS1 to produce SYN0 (2E9).

The controller I/O function lines, SR, DA, DR, and CMD, enter Sheet 2 at C1 and D1. If CTLGT (2N8) is on, indicating that the data controller or one of the files was the last I/O device addressed, these I/O functions are gated into the controller as Gated Status Request (SRG), Gated Data Available (DAG), Gated Data Request (DRG), or Gated Command (CMG).

3.5.2.2 File Addressed and File Selected

The File Addressed (FA) flip-flops are shown at 4C1. At every ADRS when the file is addressed and the write gate is not on or the controller is not busy, D101 and D111 are gated onto FA0 and FA1. FAs are decoded into FLSEL 0-3, which go to the files and select one of the four addresses.

3.5.2.3 Sense Status of File

The multiplexors at 3K6 and 3K8 have two control inputs: Enable (E) and Select (S). Control input E is always enabled (grounded). Control input S is driven by CNTAD0; thus, a status request to any file reads file status to the data lines and to the processor. The DDGRK signal (2D4) enables the buffer gates of the data lines, thus returning the address of the interrupting unit to the computer during an Acknowledge Interrupt instruction. Notice that some status lines from the files are gated in the files by File Select, while File Ready to Seek, Read, or Write, and Seek Incomplete come on separate lines from each file.

Illegal Address is stored in this controller in a separate flip-flop for each file (3H2 to 3H4). Those signals gated in the file go directly to the multiplexor at 3K6 and 3K8, while the four signals which exist as a separate line for each file are gated by the multiplexor at 3G6 to 3G9, which are controlled by File Address (FA). A Sense Status instruction addressed to any of the four files reads the status of the file addressed to the data lines and to the computer. Note that Not File Ready and Not File Ready to Seek, Read, and Write are the signals actually sent to the multiplexors; the status bits are named File Not Ready and File Not Ready to Seek, Read, or Write.

3.5.2.4 Seek and Restore Commands

The Seek and Restore controls are located between A and H of Sheet 3. When a CMD is addressed to one of the files, FLAD is set during the ADRS portion of the I/O operation. Then, when CMD is generated, D141 and D151 are gated into the Restore and Seek flip-flops, respectively (3B2 and 3B3). The Restore flip-flop sends Restore and Strobe to the file, while Seek sends Strobe only; thus, if Restore and Seek are both commanded, Restore governs. Strobe is delayed by a one-shot at 3F2 to enable Restore to settle. Strobe is gated by Write Gate, so that if head motion is commanded during Write Zero Fill, motion does not begin until Zero Fill is over. The Restore and Seek flip-flops also set Busy, causing a Controller Not Idle status. Address Acknowledge or Logical Address Interlock (Illegal Address) resets Restore and Seek, indicating that the Seek set-up is over. If the file is RSRW at this time, Seek is over; if the file is Not RSRW, Seek is in process.

3.5.2.5 Illegal Address Storage

An Illegal Address (attempt to Seek to a cylinder greater than 202) is indicated by a Logical Address Interlock (LAI) pulse (3A5) from the file currently selected. The LAI pulse sets the IA flip-flop of the selected file. The Address Acknowledge signal (ADAWK), which indicates a good Seek (or Restore) address, resets the Illegal Address flip-flop; thus, Illegal Address is reset by a legal address or by General Clear.

3.5.2.6 Interrupt Controls

Each file has its own interrupt controls and can be disarmed, enabled, or disabled independently of the other files.

3.5.2.7 Disable and Disarm Storage

The Enable, Disable, and Disarm signals are stored in the flip-flops shown at Sheet 4, Area G-H. Note the signals Enable, a positive signal, and Disarm, a ground signal.

If the file is addressed with an output command, data line bits 8 and 9 control these functions, as shown in Table 3-3.

TABLE 3-3 DATA LINE BITS 8 AND 9

DATA LINE BITS	8	9	7475 ENABLE	INPUTS ARM	FUNCTION
Binary Bits	0	0	-	-	No Change
	1	0	H	H	Disable, Arm
	0	1	L	H	Enable, Arm
	1	1	H	L	Disable, Disarm

Here, Enable permits an interrupt attention, Disable prevents an interrupt attention, and Arm permits queuing interrupt requests. Thus, Arm and Enable enable the interrupt for the file, Disable and Disarm prevent interrupts from the file, and Disable and Arm prevent interrupts, but allow storage of interrupt requests in the Queue flip-flop. General Clear forces all Enable and Arm storage flip-flops to Disable, Disarm, which is the reset condition.

3.5.2.8 File Interrupt

Each file can interrupt if:

1. the file goes Not Ready,
2. the file goes Ready to Seek, Read, or Write, or
3. seek ends.

   Seek End is signaled by:

   - FRSRW going to 0, then back to 1,
   - Address Acknowledge if FRSRW stays 1 (seek the same address),
   - Illegal Address (FRSRW stays 1), and
   - FRSRW going to C followed by Seek Incomplete (FRSRW stays 0).

Taking File 0 as typical of all four, when the file goes Not Ready, the signal FRDY01 (3K1) goes to ground, which sets the QF0 flip-flop at 3M1. If the file goes Ready to Seek, Read, or Write, the FRSRW01 signal (3J1) goes high, which sets the QF0 flip-flop. Before head motion begins in a Seek or Restore operation, FRSRW01 goes tc ground. When head motion stops normally, FRSRW01 goes high and QF0 sets as described previously.

If head motion stops improperly and a Seek Incomplete occurs, the SKINC01 signal (3J1) goes high and QF0 sets. If the Seek called for does not involve head motion, FRSRW01 stays high. An Address Acknowledge (ADAWK0) pulse (3A6) or a logical address interlock (LAI0) (3A5) occurs. These pulses are distributed to the IA flip-flops, 3H2-3H5. LAI for File 0 is ORed with ADAWK for File 0 by gate A35, shown at 3F3. The pulse from this gate goes to pin 12 of gate A36 at 3K1. If pin 13 of A36 is low, indicating that head motion occurs, pin 1 of A47 (3M1) stays high and the QF01 flip-flop does not set. If pin 13 of A36 is high, indicating that the same address is seeking and head motion does not occur, pin 1 of A47 goes low and the QF01 flip-flop sets.

A flip-flop does not get set if held reset and pulsed at the set input; if DSARM00 is low (3K1), QF01 flip-flop does not get set.

If ENBL01 (3M1) is high, the QF0 signal becomes Interrupt Request File 0 (NTRQF01) (3N1). If ENBL01 is low, the QF0 output is blocked. When the internal RACK0/TACK0 circuits (Sheet 6) respond with an Interrupt Acknowledge (INAKF00) (6N2), QF0 is reset. General Clear resets all QF flip-flops.

3.5.2.9 Internal RACK0/TACK0

If a RACK0 (2B1) signal occurs and no interrupt request from the files or the data controller is pending, the TACK0 enters at 2B1, passes through the contention circuit at 2A4, and leaves as TACK0 at 2A6.

An interrupt request from a file (NTRQFX1) or from the data controller (NTRQC1) enters at 6K1-6K4. If RACK0 is not present, the T inputs to the 7475s (6K1-6K4) are high, and the interrupt request sets the appropriate 7475. The zero outputs from the 7475s are ORed together (6N1-6N3) to produce Attention (ATEN0) to the processor and to furnish an input to the contention circuits (2A3).

When a RACK0 occurs and attention from this unit is present, TACK0 does not occur. Instead, the T inputs to the 7475s go low to prevent any more interrupt requests from disturbing the pulse gating. After a short delay (6G1), gated RACK0 pulses a priority circuit (6M1-6M4). When the delayed gated RACK0 encounters the first gate whose 7475 is set, delayed gated RACK0 becomes Interrupt Acknowledge (INAKC0 or INAKFX0), which resets the flip-flop for that device (3L1-3L5). Interrupt Acknowledge also indicates which device is being acknowledged by sending signals IAD1, IAD2 (6S5), and INAKC0 (6R1) to the multiplexors shown at 2K5-2M5. Delayed gated RACK0 is delayed again producing double-delayed gated RACK0 (DLGRK0) (6J2), which produces SYN0 (2E4-2E9) and gates the device address (2E2-2M2) to the processor.

3.5.3 Data Transfer

3.5.3.1 Data Controller Commands

Data controller commands are sent to the data controller, via CMD I/O instruction addresses, with the function desired as the output data. The command is set up in the command registers, shown at 4B5-4B7. The command is decoded and command functions are generated by subsequent gating (4E5) (4E7). Note that the format commands are disabled unless the format (FMT) switch is turned off (handle towards right). The CNTCM signal also sets the Data Controller Busy (CBSY) flip-flop (5L1).

3.5.3.2 Normal Mode Instructions

The normal mode instructions are: Read, Read-Check, and Write. Read and Read-Check are very similar and are discussed together. Normal mode assumes that the disk has been formatted. The format instructions are used to format the disk.

3.5.3.3 Track Addresses

In the process of setting up for a normal mode data transfer, the program writes data to the file, giving the cylinder address. This operation sets the file address (4C1) and loads the cylinder address into the Data Input Register (DIR) (6K6-6K9). Next, the program writes data to the data control section, giving the sector address and head. This operation transfers the cylinder address from DIR to the Data Output Register (DOR) (6M6 and 6R8) and loads the sector number and head into the DIR.

3.5.3.4 Read Operation

The program executes an output command to the data control section, with the data defining the function. Assume a read function. The output command sets CBSY (5L1). The sector comparator gates (5B8-5B9) are always operating, comparing the data from the file's internal sector counter with data from the DIR. CONTO (5D9) is described in the later sections of this chapter that deal with multisector operations; assume that it is high now. If the selected file is ready to Seek, Read, or Write (5E3) and if the data controller is Busy (5M2), a one-shot (5G3) is triggered on the trailing edge of each sector mark. Since the file's internal sector counter stops on the leading edge of sector mark, the counter has settled down by the trailing edge. This one-shot tests the output of the Sector Comparison gates, and if the sector counter and DIR agree, the Sector Comparison (SCCMP) (5H9) signal is generated. Refer to Figure 3-2 for the sector timing.

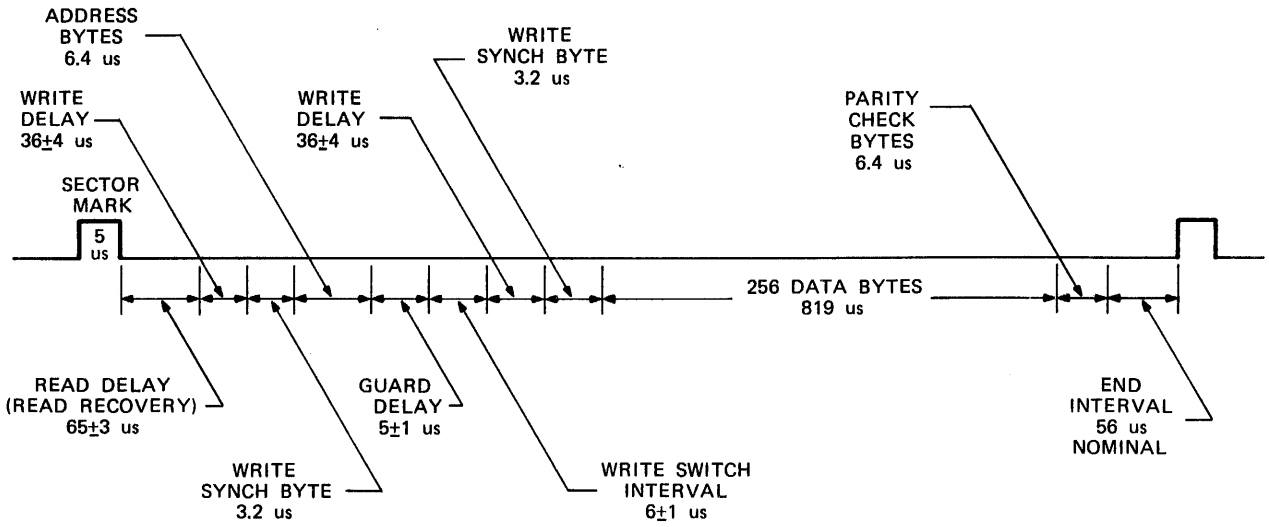


Figure 3-2 Sector Timing

3.5.3.5 Address Read

The operations Read, Read-Check, and Write should begin with an Address Read in order to verify that the sector selected is correct.

Data from the disk is received by the In Data (INDTA) flip-flop (5M9). Read Data (RDTA) from the disk first passes through a noninverting amplifier (5K9), then direct sets the INDTA flip-flop (5M9). The trailing edge of Read Clock, slightly delayed, resets INDTA. The source of data from the disk to the controller is INDTA.

If Read or Write (RDWT) is true and Sector Compare (SCCMP) occurs, the Address Read Gate (ARDGT) flip-flop (6B6) sets at the end of SCCMP (65 microseconds). ARDGT turns on Read Gate (RDGT) (5R5), and clock pulses start coming from the disk. The pattern 011 is the SYNCH pattern and is written at the beginning of each sector. The SYNCH detector gates (6A6) detect this pattern and set the Address Compare (ADCMP) (6D6) flip-flop at the trailing edge of the next Read Clock. ADCMP and Read Clock are gated together to produce Read Count Bit Counter (RCBCT) (6G5). The reset side of the compare counter flip-flop at 6E6 is gated by ADCMP and is called Compare First Byte (CMP1) (6G6). At the end of the first byte of address comparison, the trailing edge of the bit 7 signal complements the compare counter, removing CMP1. At the end of the second byte of Address Compare, the compare counter is complemented again, triggering the Address Read Complete (ARDCM) one-shot (6H7), which resets ARDGT and ADCMP, ending the address read operation.

The address comparison is accomplished with an Exclusive-OR, shown at 6F4. One input to this comparison is from the Data Auxiliary Register bit 7 (DAR7) (4N8) which is the data just received from the disk. The other input, Check Data (CKDA) (6R6) comes from the DIR and the DOR. Two 8-bit multiplexors are shown on Sheet 6. One of them, shown at 6M9, takes data from the DIR. The other, at 6R6, takes data from the DOR. The multiplexor at 6R6 is selected at all times except during the first byte of address compare. Compare First Byte (CMP1) enters at 6N5 and cuts off one multiplexor at 6R6 and turns on the multiplexor at 6M9. Since the data input register contains the sector number and head, this data is compared against data from the disk during the first byte of address read. During the second byte, CMP1 goes to 0, and the multiplexor at 6R6 is selected. Since the DOR contains the cylinder address, data from the disk is compared with the cylinder address during the second byte of address read. If the data differs, the Address Compare Error flip-flop (6F4) is set.

In addition, during the first byte of address read, the head and defective track bits from the disk are tested. At bit 3 time of CMP1 (6G6), the defective track bit is in DAR5 (4N8). If this bit is a 1, the Defective Track flip-flop (6D3) becomes set. Also at bit 3 time of CMP1, the head bit is in DAR6 (4N8). This bit is checked against the current Head Select flip-flop (HD) (4C4). If these bits differ, the Head Comparison Error flip-flop (6G4) becomes set. Note that these errors set Examine (6H3) and that Examine prevents writing on the disk (3E1). Refer to Figure 3-3 for address read and compare timing.

3.5.3.6 Read Data

An address read ends with ARDCM (6H6); the trailing edge of ARDCM triggers the Data Start (DTST) one-shot (5H7) which starts Read Data. If Combined Read (Read or Read-Check) (CRD) is present, DTST sets the Data Read Gate (DRDGT) flip-flop (5J6) which turns on the Read Gate in the selected file (5R5). Once the Read Gate is on, the controller waits for SYNCH Detected (SYNDT) (6B6), which sets the Data Read Bit Counter Gate (DRBCG) flip-flop (5N8), which gates the Read Clock to count the bit counter (6F6, 4G5).

DRDGT gates the Read Clock to produce Shift Data Input Register (SHDIR) (5N7), which shifts data from disk to the Data Input Register (DIR) (6K6, 6K8). At the end of each byte of data, bit 7 and RDGT generate Read Load Data Output Register (RLDDO1) (5N6), which shifts data from DIR to DOR (6R9, 6M6) and sets the Data Request (DTRQ) flip-flop (4F8). If this is a read operation, DTRQ passes through a gate at 4G6 and becomes DTARQ which is busy on the selector bus (3K6). If the operation is Read Check, the gate at 4G6 is closed, in which case no data request occurs.

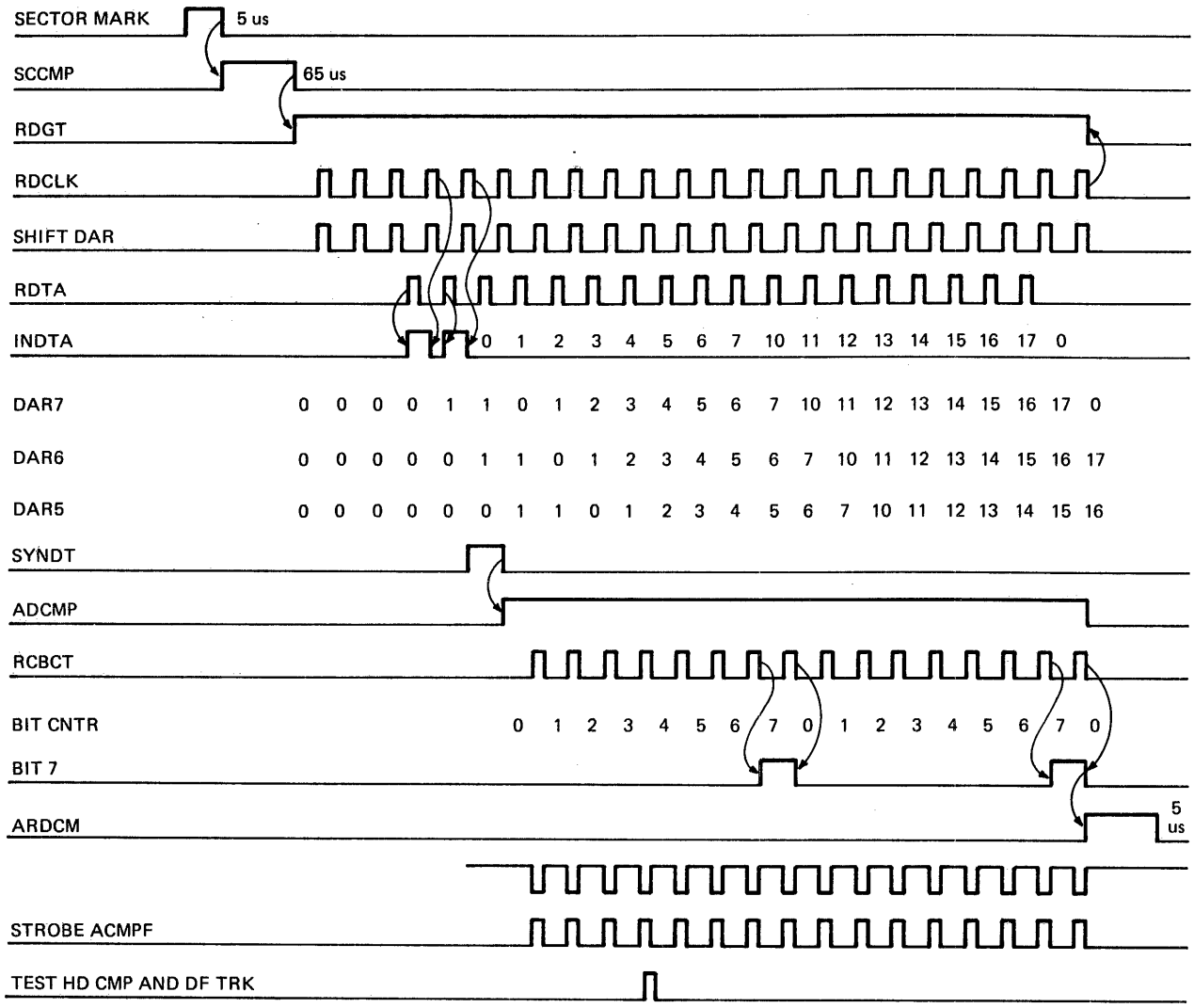


Figure 3-3 Address Read and Compare Timing

The byte counter (4K5) has been counting the bytes and at the 256th byte (byte number 255), produces the signal Byte End (BYEND) (4R3). The RLDDO at the end of the last byte sets the Cyclic Check (CKCY) flip-flop (5K6). The next RLDDO sets the Cyclic Check 2 (CKCY2) flip-flop (5L6), and the next RLDDO triggers the Read End (RDEND) one-shot (5R6).

RDEND triggers the Operation End (OPEND) one-shot (4M6). The OPEND pulse resets the five read control flip-flops (5J6-5N8). CKCYO prevents RLDDO from making a data request (4C9). If this is a single sector record, the Data Request flip-flop (4F8) should now be set, since the Selector Channel (SELCH) has not answered the last data request. The OPEND pulse passes through the gate shown at 4N7 and becomes the Operation Complete (OPCMP) pulse (4R7), which, in turn, becomes the Complete or General Clear (CMPCL) pulse (4R7), which resets CBSY (5L1), ending the Read or Read-Check operation. Refer to Figure 3-4 for read and read format timing.

For the multisector record case, refer to Section 3.5.3.12.

3.5.3.7 Longitudinal Parity Check

During a read or read-check, the longitudinal parity check circuits are operating. The longitudinal parity check shift register (6D8-6F8) is always being shifted by Write Cyclic Check (WCYCK) (6B8) except during read data, when it is shifted by the Shift Data Input Register (SHDIR) (6B8). Normally, zero is shifted through the register. During the Read Data Control (RDTAC) (6B8) time, which is between SYNCH detected and longitudinal parity check time, data from the disk, via Data Auxiliary Register 7 (DAR7), is gated into the Exclusive-OR at 6C7 and to the shift register. The other input to the Exclusive-OR is the Q output of the shift register. Through shift operations, two longitudinal parity bytes are generated. The first parity byte is an even longitudinal parity byte of odd-numbered data bytes; the second parity byte is an even longitudinal parity byte of even-numbered data bytes. Refer to Figure 3-5 for derivation of longitudinal parity bytes.

During read longitudinal parity check time, the data from the disk is compared with the data from the shift register; they should agree. If they do not agree, the J input to the Longitudinal Parity Check Error (CYER) flip-flop (6C9) goes high. This flip-flop is clocked by each read clock during parity check time, so that the flip-flop sets on longitudinal parity check error.

During write or write format operations, longitudinal parity check operates in a similar manner except that the data source is WTDTA (6B7); the shift register is shifted by WCYCK (6B8); the Longitudinal Parity Check Error (CYER) flip-flop (6C9) cannot set; and during write parity check time, the Longitudinal Parity Check Shift Register Out (CYOUT) (6F9) is written on the disk.

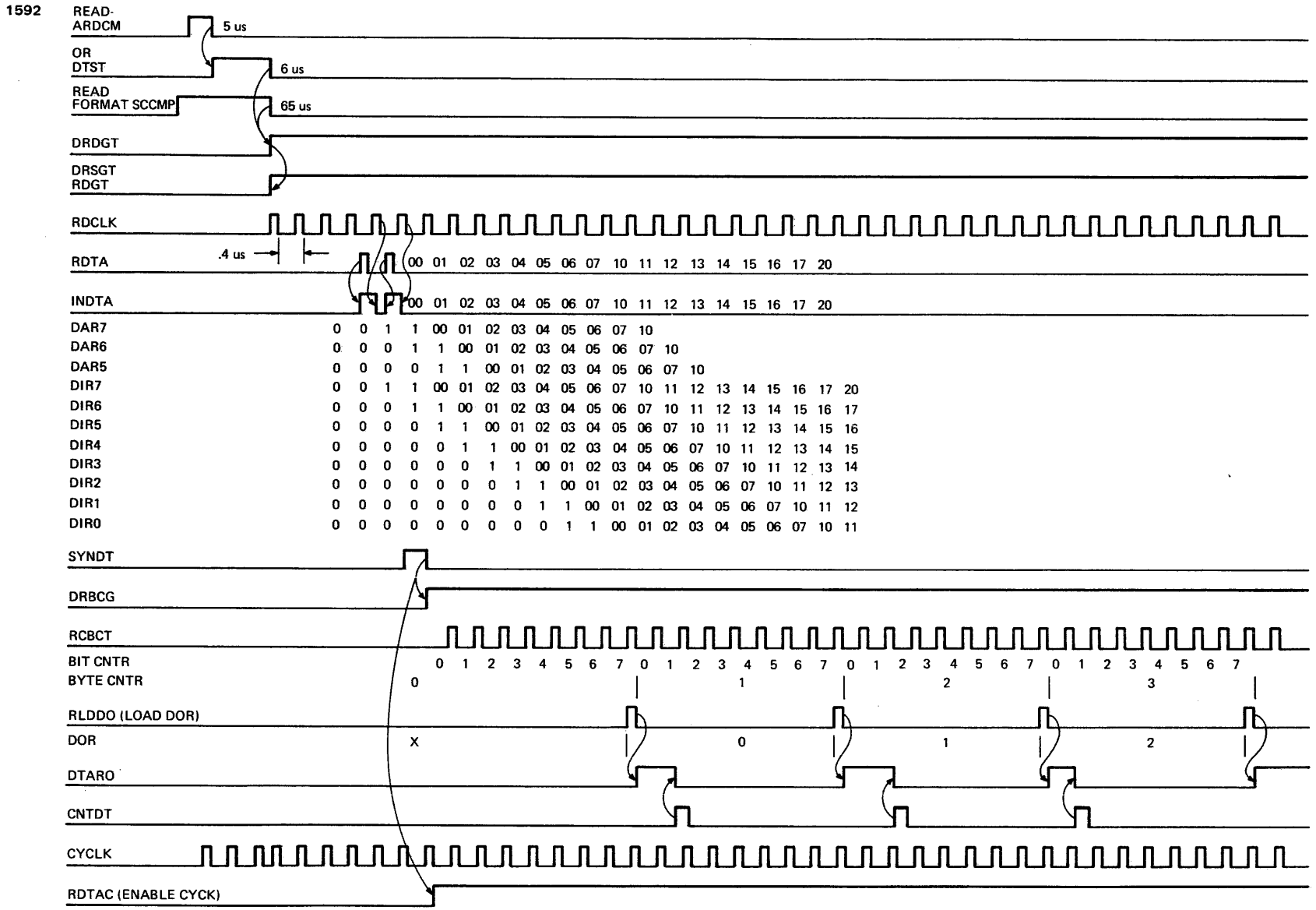
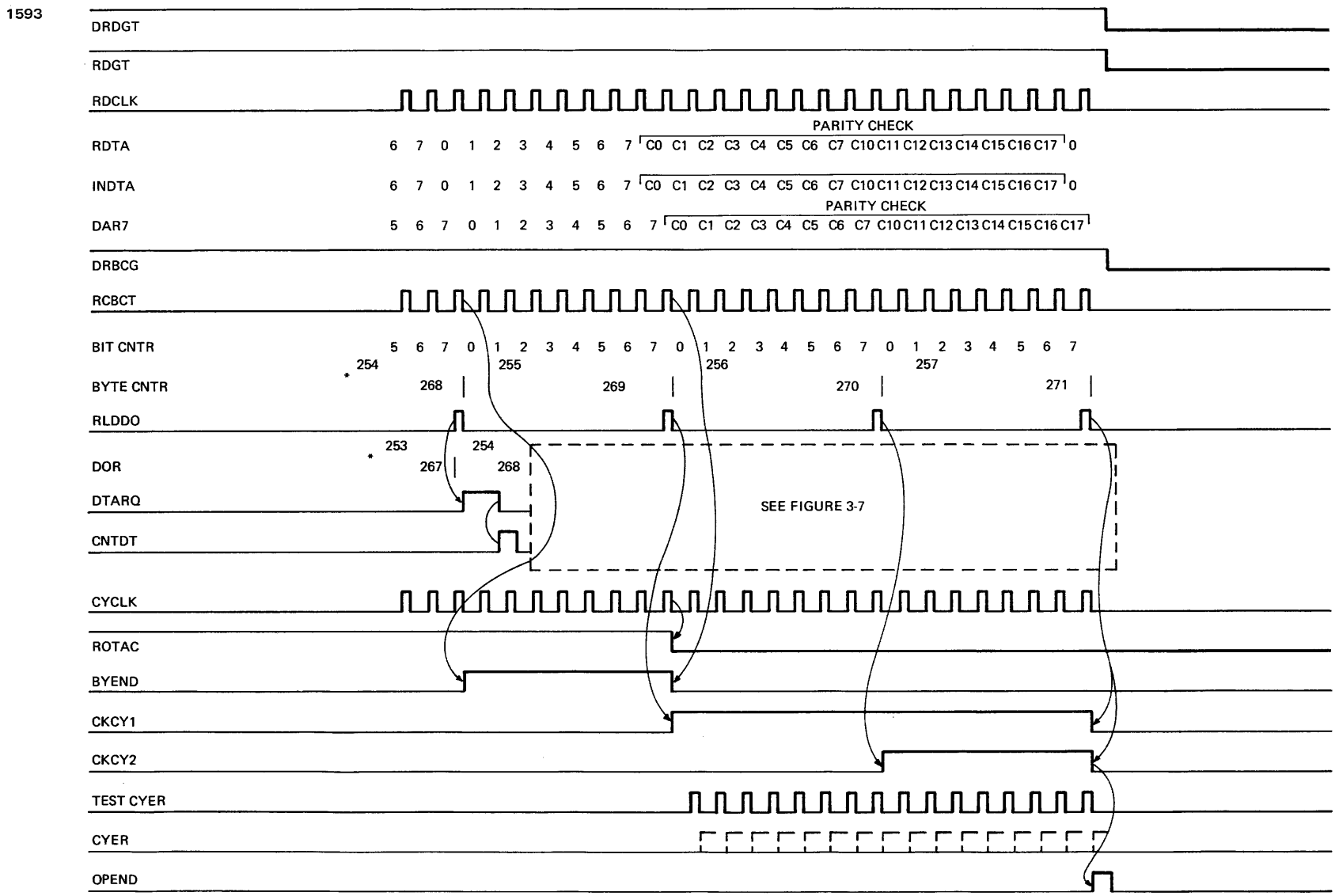
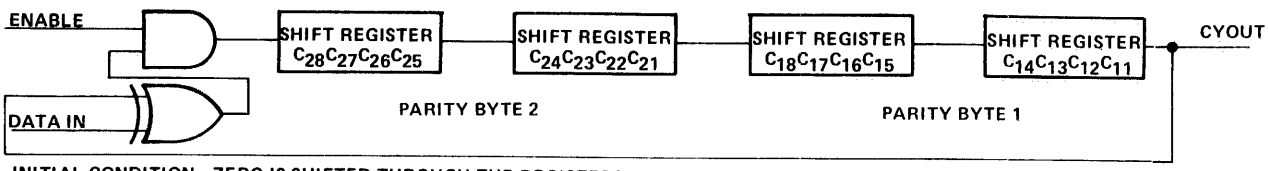


Figure 3-4 Read and Read Format Timing



*NOTE: UPPER NUMBER IS FOR READ;
LOWER NUMBER IS FOR READ FORMAT.

Figure 3-4 Read and Read Format Timing (Continued)



INITIAL CONDITION: ZERO IS SHIFTED THROUGH THE REGISTERS.
AFTER ENABLE:

BIT COUNT 1: $C_{11} = C_{12} = C_{13} = C_{14} = C_{15} = C_{16} = C_{17} = C_{18} = C_{21} = C_{22} = C_{23} = C_{24} = C_{25} = C_{26} = C_{27} = 0$;
$C_{28} = B_{11} \oplus 0 = B_{11}$

BIT COUNT 8: $C_{11} = C_{12} = C_{13} = C_{14} = C_{15} = C_{16} = C_{17} = C_{18} = 0$.
$C_{21} = B_{11} \oplus 0 = B_{11}$
$C_{22} = B_{12} \oplus 0 = B_{12}$
$C_{23} = B_{13} \oplus 0 = B_{13}$
$C_{24} = B_{14} \oplus 0 = B_{14}$
$C_{25} = B_{15} \oplus 0 = B_{15}$
$C_{26} = B_{16} \oplus 0 = B_{16}$
$C_{27} = B_{17} \oplus 0 = B_{17}$
$C_{28} = B_{18} \oplus 0 = B_{18}$

BIT COUNT 16:
$C_{11} = B_{11}$ $C_{21} = B_{21}$
$C_{12} = B_{12}$ $C_{22} = B_{22}$
$C_{13} = B_{13}$ $C_{23} = B_{23}$
$C_{14} = B_{14}$ $C_{24} = B_{24}$
$C_{15} = B_{15}$ $C_{25} = B_{25}$
$C_{16} = B_{16}$ $C_{26} = B_{26}$
$C_{17} = B_{17}$ $C_{27} = B_{27}$
$C_{18} = B_{18}$ $C_{28} = B_{28}$

BIT COUNT 17:
$C_{28} = B_{11} \oplus B_{31}$ $C_{18} = B_{21}$
$C_{27} = B_{28}$ $C_{17} = B_{18}$
$C_{26} = B_{27}$ $C_{16} = B_{17}$
$C_{25} = B_{26}$ $C_{15} = B_{16}$
$C_{24} = B_{25}$ $C_{14} = B_{15}$
$C_{23} = B_{24}$ $C_{13} = B_{14}$
$C_{22} = B_{23}$ $C_{12} = B_{13}$
$C_{21} = B_{22}$ $C_{11} = B_{12}$

BIT COUNT 32:
$C_{28} = B_{28} \oplus B_{48}$ $C_{18} = B_{18} \oplus B_{38}$
$C_{27} = B_{27} \oplus B_{47}$ $C_{17} = B_{17} \oplus B_{37}$
$C_{26} = B_{26} \oplus B_{46}$ $C_{16} = B_{16} \oplus B_{36}$
$C_{25} = B_{25} \oplus B_{45}$ $C_{15} = B_{15} \oplus B_{35}$
$C_{24} = B_{24} \oplus B_{44}$ $C_{14} = B_{14} \oplus B_{34}$
$C_{23} = B_{23} \oplus B_{43}$ $C_{13} = B_{13} \oplus B_{33}$
$C_{22} = B_{22} \oplus B_{42}$ $C_{12} = B_{12} \oplus B_{32}$
$C_{21} = B_{21} \oplus B_{41}$ $C_{11} = B_{11} \oplus B_{31}$

BIT COUNT 33:
$C_{28} = B_{11} \oplus B_{31} \oplus B_{51}$ $C_{18} = B_{21} \oplus B_{41}$
$C_{27} = B_{28} \oplus B_{48}$ $C_{17} = B_{18} \oplus B_{38}$
$C_{26} = B_{27} \oplus B_{47}$ $C_{16} = B_{17} \oplus B_{37}$
$C_{25} = B_{26} \oplus B_{46}$ $C_{15} = B_{16} \oplus B_{36}$
$C_{24} = B_{25} \oplus B_{45}$ $C_{14} = B_{15} \oplus B_{35}$
$C_{23} = B_{24} \oplus B_{44}$ $C_{13} = B_{14} \oplus B_{34}$
$C_{22} = B_{23} \oplus B_{43}$ $C_{12} = B_{13} \oplus B_{33}$
$C_{21} = B_{22} \oplus B_{42}$ $C_{11} = B_{12} \oplus B_{32}$

FINAL:
$C_{11} = B_{11} \oplus B_{31} \oplus B_{51} \oplus B_{71} \oplus \cdots \oplus B_{2551}$
$C_{12} = B_{12} \oplus B_{32} \oplus B_{52} \oplus B_{72} \oplus \cdots \oplus B_{2552}$
$C_{13} = B_{13} \oplus B_{33} \oplus B_{53} \oplus B_{73} \oplus \cdots \oplus B_{2553}$
$C_{14} = B_{14} \oplus B_{34} \oplus B_{54} \oplus B_{74} \oplus \cdots \oplus B_{2554}$

$C_{15} = B_{15} \oplus B_{35} \oplus B_{55} \oplus B_{75} \oplus \cdots \oplus B_{2555}$
$C_{16} = B_{16} \oplus B_{36} \oplus B_{56} \oplus B_{76} \oplus \cdots \oplus B_{2556}$
$C_{17} = B_{17} \oplus B_{37} \oplus B_{57} \oplus B_{77} \oplus \cdots \oplus B_{2557}$
$C_{18} = B_{18} \oplus B_{38} \oplus B_{58} \oplus B_{78} \oplus \cdots \oplus B_{2558}$

$C_{21} = B_{21} \oplus B_{41} \oplus B_{61} \oplus B_{81} \oplus \cdots \oplus B_{2561}$
$C_{22} = B_{22} \oplus B_{42} \oplus B_{62} \oplus B_{82} \oplus \cdots \oplus B_{2562}$
$C_{23} = B_{23} \oplus B_{43} \oplus B_{63} \oplus B_{83} \oplus \cdots \oplus B_{2563}$
$C_{24} = B_{24} \oplus B_{44} \oplus B_{64} \oplus B_{84} \oplus \cdots \oplus B_{2564}$
$C_{25} = B_{25} \oplus B_{45} \oplus B_{65} \oplus B_{85} \oplus \cdots \oplus B_{2565}$
$C_{26} = B_{26} \oplus B_{46} \oplus B_{66} \oplus B_{86} \oplus \cdots \oplus B_{2566}$
$C_{27} = B_{27} \oplus B_{47} \oplus B_{67} \oplus B_{87} \oplus \cdots \oplus B_{2567}$
$C_{28} = B_{28} \oplus B_{48} \oplus B_{68} \oplus B_{88} \oplus \cdots \oplus B_{2568}$

THE FIRST LONGITUDINAL PARITY BYTE EQUALS THE EVEN LONGITUDINAL PARITY BYTE OF ODD-NUMBERED DATA BYTE.
THE SECOND LONGITUDINAL PARITY BYTE EQUALS THE EVEN LONGITUDINAL PARITY BYTE OF EVEN-NUMBERED DATA BYTE.

Figure 3-5 Derivation of Longitudinal Parity Bytes

3.5.3.8 Write Data

Write Data begins with Address Read. Address Read ends with Address Read Complete (ARDCM), which triggers the Data Start (DTST) one-shot (5G7).

DTST and Write (WT) become Write Start (WTST) (5H8). WTST sets the Write Gate (WTGT) flip-flop (5K3) and produces a Write Load Data Output Register (WLDOR) pulse (5S4) which generates a data request (4G6), requesting the first byte from SELCH and loading it into the Data Input Register (DIR) (6K6-6K8).

The Write Gate flip-flop turns on Write Gate (WTGT) to the file (3F1) and enables Write Zeros (5S4), thus writing a string of zeros on the disk.

The write oscillator (2F8) produces pulses at 6.248 MHz. These pulses toggle a flip-flop at 2G8, which produces a 3.124 MHz square wave. This square wave (WTOSC) (2K8) toggles the Phase flip-flop (5J4). This flip-flop is reset during the Write Clock phase and is set during the Write Data phase. Each phase is 320 nanoseconds long, and a bit cell is 640 nanoseconds long. WTGT enables Write Phase to Write Clock and Data which is gated with WTOSC (5R4), producing pulses 160 nanoseconds long, which are sent to the file.

WTST also triggers the Write Delay (WTDLY) one-shot (5G4). The trailing edge of WTDLY sets the Write Bit Counter Gate (WBTCG) flip-flop (5L3).

WBTCG turns Erase Gate on (3E2) and gates Write Clock to form Write Count Bit Counter (WCBCT) (5S3), which is counted by the bit counter (4J5).

Write Bit Counter Gate also enables the Enable SYNCH (ENSYN) signal (5S3). ENSYN and bit counters B2 and B4 (5J5), which are true only during bit counter times 6 and 7, pass through an OR gate (5M5). They are then gated by data phase (5N5) and ORed with Clock to produce Write Clock and Data, which are gated by WTOSC to produce Write Data and Clock (WTDAC) (5S4) for the file. This signal, present only during bit times 6 and 7 of Enable SYNCH, writes the ones of the SYNCH byte.

During bit counter 7 time, the bit 7 signal occurs. This signal is gated with WTCLK to produce Write Gated Bit 7 (WGBT7) (5N4). WGBT7 shifts the shift register shown at 4B9, which is now shifting zeros. WGBT7 and WBTCG (5M2) produces Write Load Data Output Register (WLDOR) (5S4); WGBT7 and WBTCG also set the Data Out flip-flop (5N3), which removes ENSYN (5S3) and produces Enable Data (ENDTA) (5S2).

WLDOR (5S4) shifts the byte in DIR to DOR (6M6-6R9) and sets Data Request (4F8). Data Request is sent to SELCH as Not Busy (3K6). SELCH responds with the next byte on the data lines and sends a DA signal, which is accepted as DAG and generates SYN (2E9). DAG also becomes CNTDT (2S7), which resets Data Request (4G6).

The content of DOR is multiplexed to become Data Output Register Out (DOROT) (6R7). The multiplexor is driven by the bit counter bits (B1, B2, and B4) (6S9). DOROT is gated by ENDTA (5J6) to produce Write Data (WTDTA) (5L6), which becomes data to the disk.

This process continues. Data is continually multiplexed from DOR to the disk. At the end of each byte, the next byte is moved from DIR to DOR, and the SELCH furnishes the third byte to DIR.

The byte counter counts the bytes (4K5-4N5) and, at the 256th byte, (byte number 255) generates the signal BYEND into the last byte (LSTBY) flip-flop, which is the first flip-flop of the shift register shown at 4B9. The last byte circulates back to the input to the shift register sc that ones are now shifted down the shift register.

At the end of the next byte, Write Last Byte (WLSBY) (4C7) goes to one. WLSBY turns off ENDTA (5S2), stopping data output to the disk, and turns on Enable Longitudinal Parity Check (ENCY), which feeds the output of the longitudinal parity check shift register (CYOUT) (5J5) to the disk.

The next WGBT7 pulse shifts a one to the next flip-flop (4B9), whose output is not used. This flip-flop provides for two bytes of longitudinal parity check data.

The next WGBT7 sets the Write End (WTED) flip-flop (4B8). WTED turns off ENCY; therefore, no more data is sent to the disk. Clock pulses continue to be written, however, filling the sector with zeros.

WTED also triggers the Operation End (OPEND) one-shot (4L6). This results in CMPCLR (4R7), as previously explained in Read Data, and in Sector Mark, End, or General Clear (SECLR) (5K3), resetting all write control flip-flops except Write Gate, which is reset by Sector Mark or General Clear (SMCLR) (5H2). Since the Write Gate flip-flop stays on, Zero Fill continues until the next sector mark. Refer to Figure 3-6 for Write and Write Format timing.

3.5.3.9 Read Format

Read Format is identical to Read Data except for starting and ending. Since Read Format does not include an Address Read operation, it is started by Sector Compare (SCCMP) (5H9). SCCMP sets the flip-flop shown at 5J7 while the Read Format (RDFOT) signal is present. The output from this flip-flop becomes Data Read Data Gate (DRDGT) (5L7). From this point, Read Format is the same as Read except that BYEND (5S2) occurs at the 270th byte (byte number 269). Refer to Figure 3-4 for Read and Read Format timing.

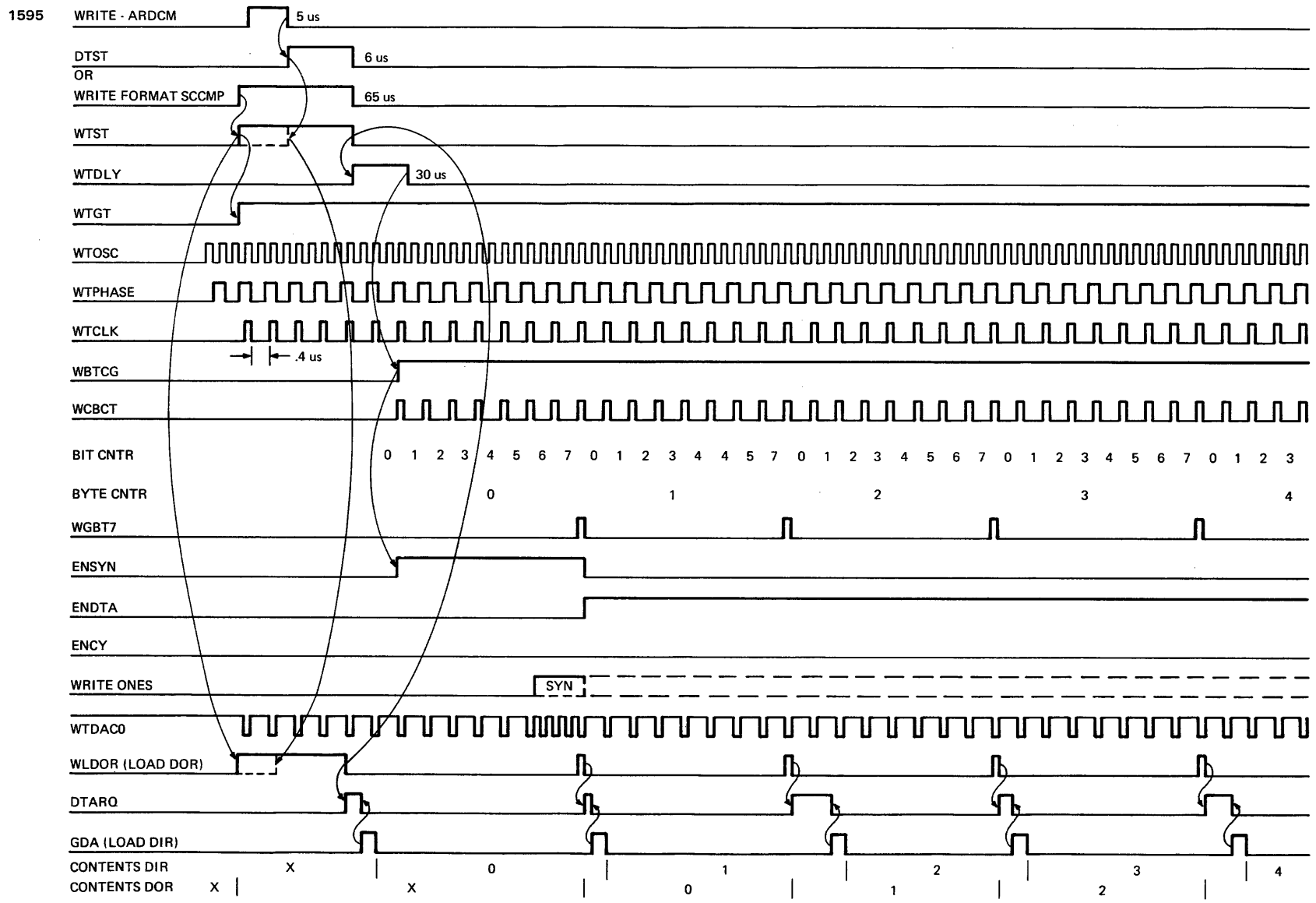


Figure 3-6 Write and Write Format Timing

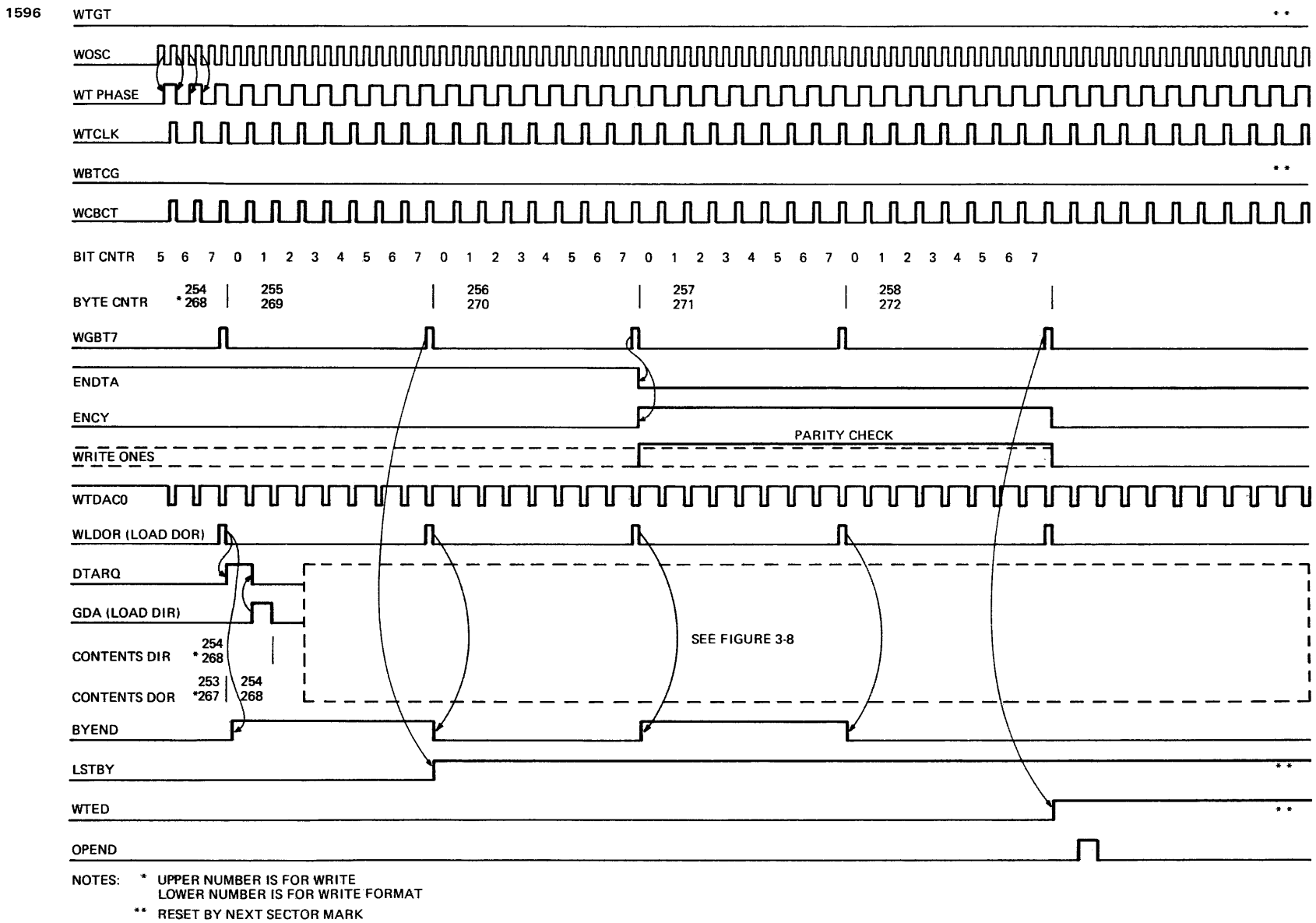


Figure 3-6 Write and Write Format Timing (Continued)

3.5.3.10 Write Format

Write Format is identical to Write Data except for starting and ending. Since Write Format does not include an Address Read operation, it is started by Sector Compare (SCCMP) (5H9). The Write Format command (WTFOT) (5G9) and SCCMP are ANDed together (5G9) and then ORed with the Write Normal Start to form the Write Start (WTST) signal (5G7). The remainder of Write Format is identical to Write, except that BYEND (5S2) is generated by the 270th byte (byte number 269). Refer to Figure 3-6 for Write and Write Format timing.

3.5.3.11 Format Mode Errors

Since format mode operations do not include the Address Read operation, the errors associated with Address Read, Address Compare Error, and Defective Track cannot occur; however, longitudinal parity error can occur.

3.5.3.12 Multisector Records

The disk controller can transfer data into records which extend over more than one sector.

The end of data transfer is determined by the SELCH. The only way to determine if the SELCH has finished is by trying to transfer another byte. If the SELCH responds with DA or DR, it has not ended.

There are three cases:

- SELCH stops before the sector ends.
- SELCH stops at the same time the sector ends.
- SELCH has more data to transfer when the sector ends.

The last case is the continue case; data remains after the sector is over and the data transfer operation must continue into the next sector.

3.5.3.13 Read Multisector

At the beginning of Read Longitudinal Parity Check, near the end of a Read operation, CKCY1 (5L6) is set by RLDD01 (5N6). That same RLDD0 sets Data Request (4F8) and also sets CKCY2 (5M7). CKCY0 (4C9) prevents further data requests (4G6). If SELCH responds with DR, CNTDT resets Data Request (4F8). The 0 output of Data Request remains low until passing the sector boundary, so the J input of the Continue flip-flop (4H7) stays high. On the leading edge of CKCY20 (4C7), the Continue flip-flop is set, indicating that more data remains to be transferred.

If CONT is set, Sector Compare is forced (5D9), Address Compare is disabled (6E5), and a Read or Read Format operation is started for the next sector. Operation continues in the new sector in the same manner as described for a one sector operation. Refer to Figure 3-7 for Read Multisector timing.

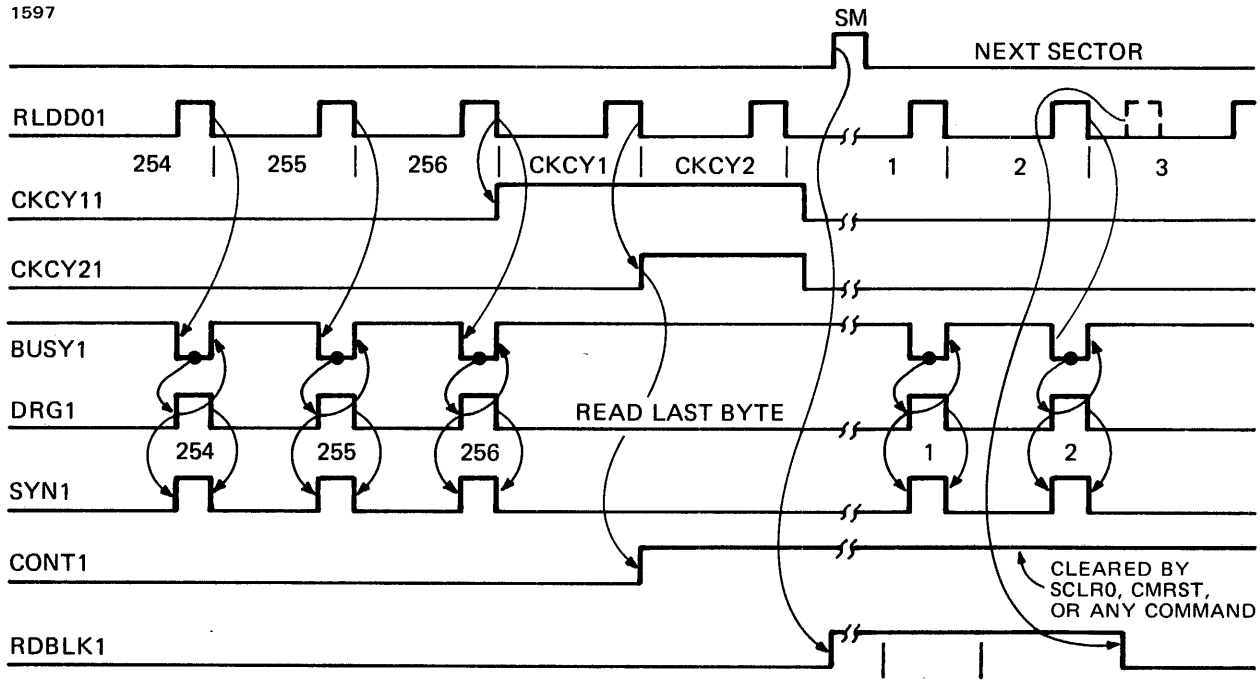


Figure 3-7 Multisector Read and Read Format Timing

3.5.3.14 Write Multisector

Near the end of a Write or Write Format operation, the signal Last Byte (LSTBY) (4C8) occurs during the last data byte before the parity check is written. It is set on the leading edge of WGBT71 (4A9). LSTBY1, ANDed with BYENDO (4C8), blocks further data requests. Data Request is set on the trailing edge of WLDOR (4D7).

If SELCH has ended, it does not send a DA; therefore, DTRQ (4F7) does not reset. WTED (4K6) triggers OPEND (4M6) which, if DTRQ is set, becomes OPCMP (4R7), ending the operation.

If SELCH has not ended, it responds with DA, which clears DTRQ (4F7). END1 (4K7) stays low and blocks OPEND (4N7) and CMPCL (4R7) does not occur. In this case WLSBY (4C7) sets Continue (CONT) (4H7). At the beginning of the next sector, SCCMP is forced (5H9) and address comparison is inhibited (6E5). Write or Write Format continues as described previously. Refer to Figure 3-8 for Write Multisector timing.

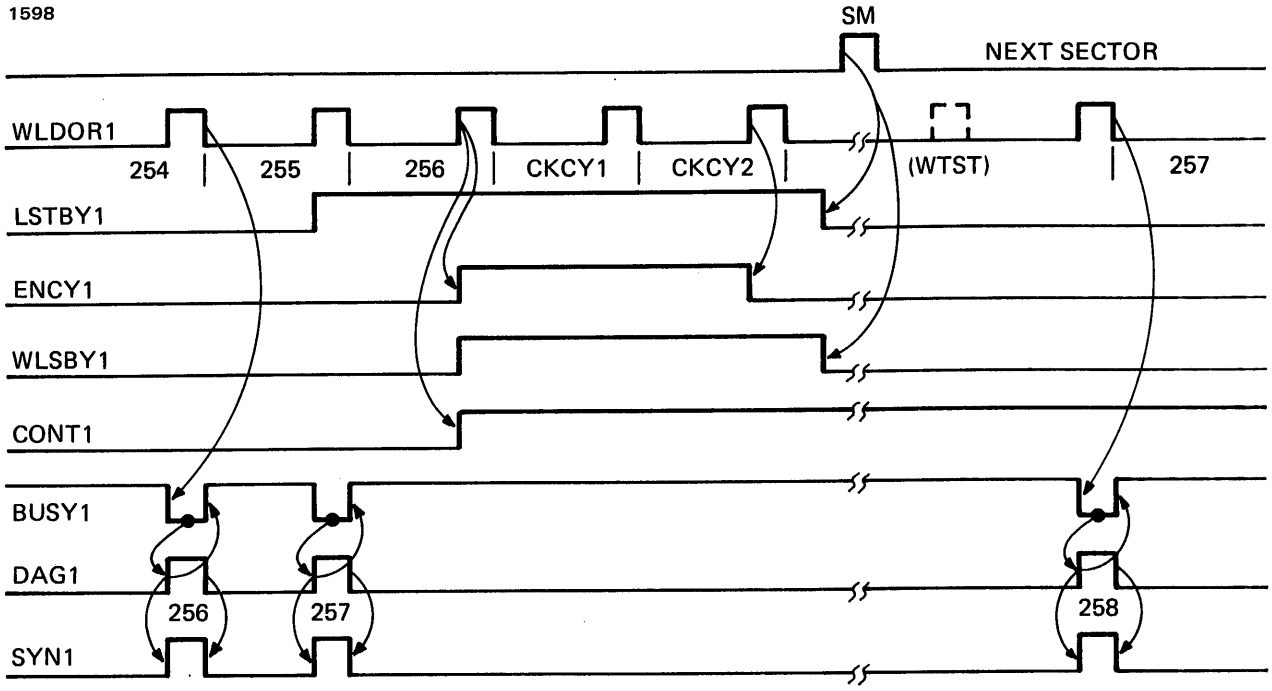


Figure 3-8 Multisector Write and Write Format Timing

3.5.3.15 Automatic Head Switch

When in a multisector record, it may be necessary to switch from head 0 to head 1.

The Index Store (IDXST) flip-flop (5F1) is set by the Index Mark and reset by the trailing edge of the first Sector Mark (SM) after Index (5F2). The AND of IDXST, Sector Mark and Continue (XSMC) (4K8), sets the Head (HD) flip-flop (4C4). This can only occur if Continue is set, indicating more data, and at the first Sector Mark after Index. If HD is already set, it does not change; instead, the signal Index Store, Sector Mark, and Continue (IXSMC) (6A2) set the Cylinder Overflow (CYLOF) flip-flop (6D2). CYLOF appears as an error and sets Examine (6H2). Examine inhibits Write (3E1), so that data on the disk is not changed.

3.5.3.16 Bit and Byte Counters

The bit and byte counters are combined in one 12-bit counter. The three least significant bits are the bit counter; the remainder is the byte counter. The counters are cleared by General Clear, Sector Mark, and Data Start (4G6); they count Write Count Bit Counter (WCBCT) and Read Count Bit Counter (RCBCT) (4G5) pulses. The outputs of the bit counter flip-flops are named B1, B2, and B4 (4J2). The bit counter is decoded to give two signals, bit 3 (4L2) and bit 7 (4L2). The byte counter is decoded to give two signals, byte 269 (BY 269) (4L3) and byte 255 (4N3). These signals are used to signal the end of a sector. CNT5 (4M3), which indicates that a Format command is being executed, selects BY 269; otherwise, BY 255 is selected.

3.5.3.17 Track Address

The Track Address (TA) drivers are shown at 5C5-5C7. Track Address comes from DIR (6K6-6K9).

3.5.3.18 Errors

Errors associated with Address Read are discussed in the section on Address Read; Cylinder Overflow is discussed in the section on Automatic Head Switch. Overrun is the only other error. Overrun (6D4) is set whenever at least one full disk revolution has passed since a data controller command and no Sector Compare (SCCMP) has occurred. The two counter flip-flops (6D4) are held reset when the data controller is not busy (CBSY) (6B5). When the data controller goes busy, the counters count Index Store (IDXST) (6C5), which goes true at index and false at the end of the first sector mark after index. If Sector Compare occurs, it resets the counters. The second flip-flop can be set by the first, but not reset. The usual cause of overrun is calling for a sector number which is too large for the disk. Refer to Figure 3-9 for Read and Write Gate on-off timing.

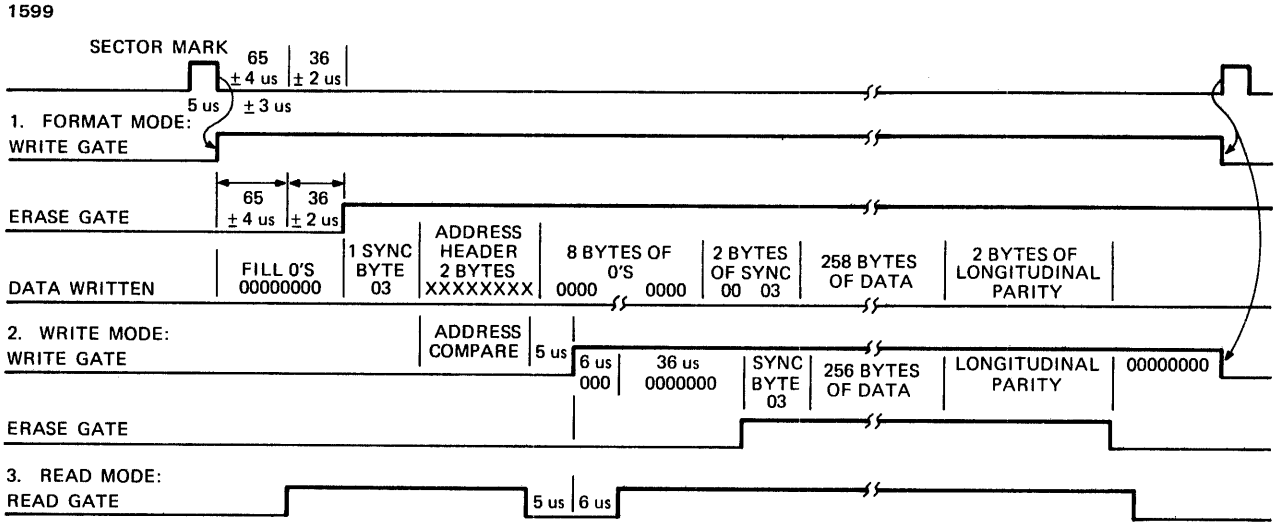


Figure 3-9 Read and Write Gate On-Off Timing

3.6 MNEMONICS

The following list identifies each mnemonic found in the Vanguard I (10 Mb) Removable Cartridge Disk System. The source of each signal on Functional Schematic 02-263D08 is also provided.

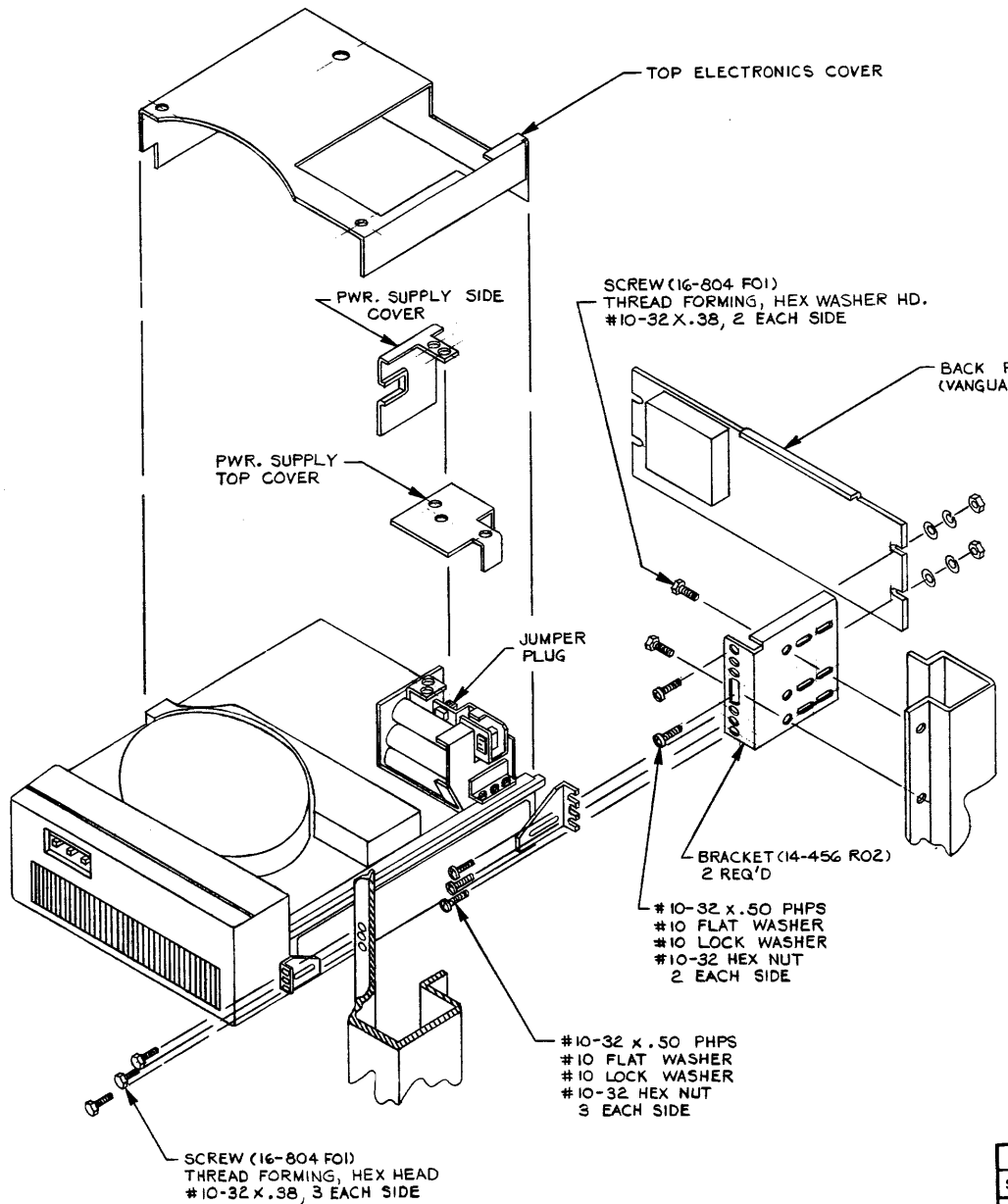
MNEMONIC	MEANING	LOCATION
ACMPF1	Address compare failure	6H4
ADAWK0	Address acknowledge	3A6
ADAWK1	Address acknowledge	3C6
ADRS0	Address	2F1
ADRS1	Address	2F3
ARDCM0	Address read complete	6H7
ARDGT0	Address read gate	6B6
ATEN1	Attention	6N1
ATN0	Attention	2A1
B11	Bit counter bit 1	4J2
B21	Bit counter bit 2	4J2
B41	Bit counter bit 4	4J1
BIT 31	Bit counter equals 3	4L2
BIT 71	Bit counter equals 7	4L2
BUSY0	Busy	3G3
BUSY1	Busy	3E3
BYEND0	Byte end	5S2
BYEND1	Byte end	4R3
CBSY1	Controller busy	5M2
CEXAM0	Controller examine	6H2
CEXAM1	Controller examine	6H3
CKCY0	Cyclic check	5S7
CKCY1	Cyclic check	5L6
CKCY20	Cyclic check two	5M7
CKDA1	Check data	6R6
CL070	Power failure clear	3E1
CMD0	Command	2C1
CMG0	Gated command	2C9
CMP11	Compare byte 1	6G6
CMPCL0	Completed or general clear	4R7
CNT50	Control 5 (A format command)	4C5
CNT51	Control 5 (A format ccmmand)	4D5
CNTAD0	Controller addressed	2M8
CNTAD1	Controller addressed	2M7
CNTCM0	Controller command	2S8
CNTCM1	Controller command	5M1
CNTDT0	Controller data transfer	2S7
CONT0	Continue	4H8
CRD1	Combined read command (read or read check)	4E6
CTLGT1	Control gate	2N8
CY2561	Cylinder address 256	6K5
CYLOF1	Cylinder overflow	6E2
CYOUT1	Cyclic out	6G9
D<080:150>	Data lines 8:15	2M1,2G1
D<080A:150A>	Data lines 8:15	2M4,2G4
D<081:151>	Data lines 8:15	2M4,2G4

MNEMONIC	MEANING	LOCATION
DA0	Data available	2C1
DAG0	Gated data available	2C9
DAR41	Data auxiliary register bit 4	4N9
DAR51	Data auxiliary register bit 5	4N8
DAR61	Data auxiliary register bit 6	4N8
DAR71	Data auxiliary register bit 7	4N8
DAT<081:151>	Data bits 8:15	3S6,3S8
DATAOV1	Data overflow	4H9
DDGRK0	Double delayed gated RACK0	6J2
DFTRK1	Defective track	6E3
DIR<001:031>	Data input register bits 0:3	6L8
DIR<041:071>	Data input register bits 4:7	6M8
DISARM00	Disarm disk 0	4H1
DISARM10	Disarm disk 1	4H2
DISARM20	Disarm disk 2	4H3
DISARM30	Disarm disk 3	4H3
DOR<001:031>	Data output register bits 0:3	6N7
DOR<041:071>	Data output register bits 4:7	6R8
DORCT1	Data output register out	6R7
DR0	Data request	2D1
DRBCG0	Data read bit counter gate	5S8
DRBCG1	Data read bit counter gate	5S8
DRDGT0	Data read gate	5L7
DRDGT1	Data read gate	5L8
DRG0	Gated data request	2D9
DSKSEL0	Disk select	4C2
DTARQ0	Data request	4G6
DTST0	Data start	5H7
DTXFER1	Data transfer error	6C1
ENBL01	Interrupt enable disk 0	4H1
ENBL11	Interrupt enable disk 1	4H2
ENBL21	Interrupt enable disk 2	4H4
ENBL31	Interrupt enable disk 3	4H3
END1	End	4G8
ENDTA0	Enable data	5S2
ENSYN1	Enable SYNC	5S3
ERSGT0	Erase gate	3F1
FA00	File address	4C1
FA01	File address	4C1
FA10	File address	4C1
FA11	File address	4C1
FILE1	File	2K9
FLAD1	File addressed	2M8
FLSEL00	File selected disk 0	4E1
FLSEL10	File selected disk 1	4E1
FLSEL20	File selected disk 2	4E1
FLSEL30	File selected disk 3	4E2
FRDY00	File ready disk 0	3A7
FRDY10	File ready disk 1	3A7
FRDY20	File ready disk 2	3A8
FRDY30	File ready disk 3	3A8
FRDY0	File ready	3H7
FRDY01	File ready disk 0	3C7

MNEMONIC	MEANING	LOCATION
FRDY21	File ready disk 2	3C8
FRDY31	File ready disk 3	3C8
FRSRW00	File ready to seek, read, or write disk 0	3D6
FRSRW10	File ready to seek, read, or write disk 1	3D6
FRSRW20	File ready to seek, read, or write disk 2	3D6
FRSRW30	File ready to seek, read, or write disk 3	3D7
FRSRW01	File ready to seek, read, or write disk 0	3F6
FRSRW11	File ready to seek, read, or write disk 1	3F6
FRSRW21	File ready to seek, read, or write disk 2	3F6
FRSRW31	File ready to seek, read, or write disk 3	3F7
FRSRW1	File ready to seek, read, or write	3H6
GCLR0	General clear	2S6
GCMD1	Gated command	2R8
HD0	Head 1 selected	4C4
HD1	Head 1 selected	4C3
HDSEL0	Head select	3C1
HIDEN0	High density	5F5
HIDEN1	High density	5G5
IA01	Illegal address disk 0	3H2
IA11	Illegal address disk 1	3H3
IA21	Illegal address disk 2	3H3
IA31	Illegal address disk 3	3H4
IAADWK00	Illegal address or address acknowledge disk 0	3F3
IAADWK10	Illegal address or address acknowledge disk 1	3F3
IAADWK20	Illegal address or address acknowledge disk 2	3F4
IAADWK30	Illegal address or address acknowledge disk 3	3F4
IAD11	Interrupt address 1	6S5
IAD21	Interrupt address 2	6S5
IDXST1	Index pulse stcre	5G1
INAKC0	Interrupt acknowledge controller	6R1
INAKF00	Interrupt acknowledge disk 0	6N2
INAKF10	Interrupt acknowledge disk 1	6R3
INAKF20	Interrupt acknowledge disk 2	6N3
INAKF30	Interrupt acknowledge disk 3	6R4
INDTA1	In data	5S9
INDTA1A	In data	5N9
INDX0	Index mark	5A1
INDX0A	Index mark	5F1
IXSMC	Index-sector mark-continue	4K8
IXSMC0A	Index-sector mark-continue	6C2

MNEMONIC	MEANING	LOCATION
LAIO	Logical address interlock	3A5
LSTBY1	Last byte	4C8
NTRQC1	Interrupt request controller	5R1
NTRQF01	Interrupt request disk 0	3N1
NTRQF11	Interrupt request disk 1	3N2
NTRQF21	Interrupt request disk 2	3N4
NTRQF31	Interrupt request disk 3	3N5
OPCMP0	Operation completed	4R7
OPEND0	Operation end	4M7
OVERRUN	Overrun	6D4
PREAM	Preamble	5H3
RACK0	Receive acknowledge	2B1
RACK0A	Receive acknowledge	2B6
RCBCT0	Read count bit counter	6G5
RD256END0	Read 256 byte ended	4J9
RDBLK0	Read block	4K6
RDCLK0	Read clock	5J9
RDCLK1	Read clock	5J9
RDEND0	Read end	5S6
RDFOT1	Read format	4F4
RDGT0	Read gate	3C1
RDGT1	Read gate	5R5
RDRFT1	Read or read format	4F5
RDTA0	Read data	5J9
RDTAC0	Read data control	5S7
RDWT1	Read or write	4F7
RLDD00	Read load data output register	6K5
RLDD01	Read load data output register	5N6
RSTR0	Restore	3D2
SCCMP0	Sector compare	5H9
SCCMP1	Sector compare	5H9
SCLR0	System clear	2E1
SCLR0A	System clear	2E4
SEC10	Sector counter bit 1	5A2
SEC20	Sector counter bit 2	5A2
SEC40	Sector counter bit 4	5A3
SEC80	Sector counter bit 8	5A3
SEC160	Sector counter bit 16	5A4
SEC320	Sector counter bit 32	5A4
SEC11	Sector counter bit 1	5C2
SEC21	Sector counter bit 2	5C2
SECLR0	Sector mark + operation completed + general clear	5K3
SHDIR0	Shift data input register	5N7
SKINC00	Seek incomplete disk 0	3D7
SKINC10	Seek incomplete disk 1	3D8
SKINC20	Seek incomplete disk 2	3D8
SKINC30	Seek incomplete disk 3	3D8
SKINC01	Seek incomplete disk 0	3F7
SKINC11	Seek incomplete disk 1	3F8
SKINC21	Seek incomplete disk 2	3F8

MNEMONIC	MEANING	LOCATION
SKINC31	Seek incomplete disk 3	3F8
SKINC1	Seek incomplete	3K7
SM0	Sector mark	5A2
SM1	Sector mark	5E3
SMCLR0	Sector mark + general clear	5H2
SR0	Status request	2D1
SREQ0	SELCH request	2A1
ST<081:151>	Status bits 8:15	3M8,3M6
STCLR0	Controller start or general clear	5R1
STRB0	Strobe	3H1
SYN0	SYNC to computer	2E9
SYNDT1	SYNC character detected	6B6
TA10	Track address 1	5C4
TA20	Track address 2	5C5
TA40	Track address 4	5C5
TA80	Track address 8	5C5
TA160	Track address 16	5C6
TA320	Track address 32	5C6
TA640	Track address 64	5C7
TA1280	Track address 128	5C7
TA2560	Track address 256	5C7
TACK0	Transmit acknowledge	2A6
THERM0	Terminate	2B1
WAWFT1	Write or write format	4E6
WBTCG1	Write bit ccunter gate	5M2
WCBCT0	Write count bit counter	5S3
WCYCK	Write clock	5S5
WGBT71	Write gated bit 7	5N4
WLDOR	Write load data output register	5S4
WLDOR0	Write load data output register	5G8
WLSBY1	Write last byte	4C7
WRTCK0	Write check	3A6
WRTCK1	Write check	3C6
WT1	Write command	4F6
WTCLK1	Write clock	5M3
WTDAC0	Write data and clock	5S4
WTDTA0	Write data	5L6
WTED0	Write end	4D8
WTFOT1	Write format	4F5
WTGT0	Write gate	3F1
WTGT0A	Write gate	3G1
WTGT0A-CBSY0	Write gate + controller busy	3K9
WTGT1	Write gate	5L2
WTPT0	Write protect	3A6
WTPT1	Write protect	3C6
WTST0	Write start	5H8
XFER1	Transfer	2C7
Y11	Byte counter bit 1	4K3
Y21	Byte counter bit 2	4K4
Y41	Byte counter bit 4	4K4
Y81	Byte counter bit 8	4K4
Y161	Byte counter bit 16	4M4



VOLTAGE CONVERSION PROCEDURE:

1. REMOVE AC CORD FROM POWER SUPPLY.
2. REMOVE THREE HOLD-DOWN SCREWS; REMOVE TOP ELECTRONICS COVER.
3. REMOVE TWO SIDE COVER SCREWS AND MOVE COVER AWAY FROM POWER SUPPLY.
4. REMOVE REMAINING POWER SUPPLY TOP COVER SCREW AND LIFT COVER WITH ATTACHED CIRCUIT BREAKERS TO THE REAR
5. REPLACE P28 (WHITE NYLON JUMPER PLUG) WITH APPROPRIATE JUMPER PLUG:
   A. 115VAC 17-552 F01
   B. 230VAC 17-552 F02
6. REASSEMBLE POWER SUPPLY.
7. REPLACE AC CONNECTOR WITH APPROPRIATE TYPE:
   A. 115VAC 26-248
   B. 230VAC 26-266
8. MAKE ALL NECESSARY CHANGES TO THE LABELS ON THE DRIVE TO REFLECT THE VOLTAGE CHANGES.

REVISIONS		
PRE PRODUCTION APPROVAL	INIT	DATE
DEV	CDB	11-7-80
PROD	[illegible]	11/7/80

RELEASED FOR PRODUCTION
MFG. ENG. MJX DATE 4/20/81

NOTES

UNLESS OTHERWISE SPECIFIED			
SCALE:	TOLERANCE:		
DIMENSIONS ARE IN INCHES	.XXX ± .003	.X ± .03	ANGLES ± 1°
	.XX ± .02		

NAME	TITLE	DATE
A. WILLIAMS	DES / DFT	9-16-80
H. MATTER	SUPV	4-13-81
	CHK	
C. BRANDT	ENG	4-13-81
	MGR	
R. BARKER	QC	4-13-81

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

TITLE
INSTALLATION AND VOLTAGE CONVERSION, VANGUARD I

TASK DATA	SHT
DWG 02-708 C12	1 - 1

SHEET LOCATION	ROW 2	TERM. NO.	ROW 1	SHEET LOCATION
3A6	WTPTO	24	*SKINC00	3D7
3A6	WRTCKO	23	* FRDY00	3A7
	GND	22	RDGTO	3C1
	GND	21	*FRSRW00	3D6
3A6	ADAWKO	20	LAIO	3A5
	GND	19	RSTRO	3D2
	GND	18	HDSELO	3C1
3F2	ERSGTO	17	WTGTO	3F1
	GND	16	STRBO	3J1
	GND	15	RDTAO	5J9
	GND	14	INDXO	5A1
	GND	13	SMO	5A2
	GND	12	SEC40	5A3
5A2	SECIO	11	SEC20	5A2
5A4	SEC320	10	SEC80	5A3
	GND	09	SEC160	5A4
	GND	08	RDCLKO	5J9
	GND	07	WDTACO	5S4
	GND	06	TA640	5C7
5C7	TA2560	05	TA1280	5C7
5C5	TA20	04	TA40	5C5
5C5	TA80	03	TA10	5C4
	GND	02	TA160	5C6
5F5	HIDENO	01	TA320	5C6
4C2	DSKSELO	00	* FLSELO	4E1

CONN 3

SHEET LOCATION	ROW 2	TERM NO.	ROW 1	SHEET LOCATION
	GND	00	FRSRW10	3D6
		01	FRDY10	3A7
		02	SKINC10	3D8
		03	FLSEL10	4E2
		04	GND	
		05	FRSRW20	3D6
		06	FRDY20	3A8
		07	SKINC20	3D8
		08	FLSEL20	3D8
		09	GND	
		10	FRSRW30	3D7
		11	FRDY30	3A8
		12	SKINC30	3D8
		13	FLSEL30	4E2
	GND	14	GND	

CONN 2

SHEET LOCATION	ROW 1	TERM. NO.	ROW 2	SHEET LOCATION
	P5	41	GND	
	GND	40	GND	
		39		
		38		
		37		
		36		
		35		
		34		
		33		
		32		
		31		
		30		
		29		
		28		
		27		
2E1	SCLRO	26		
		25	SREQO	2A1
2D1	XFERO	24	TERMO	2B1
2E9	SYNO	23	ATNO	2A1
2B1	RACKO	22	TACKO	2B7
3E1	CLO70	21	DAO	2C1
2D1	DRO	20	CMDO	2C1
2D1	SRO	19	ADRSO	2F1
2H1	DI40	18	DI50	2G1
2J1	DI20	17	DI30	2H1
2L1	DI00	16	DI10	2K1
2M1	DO80	15	DO90	2L1
		14		
		13		
		12		
		11		
		10		
		09		
		08		
		07		
		06		
		05		
		04		
		03		
		02		
	GND	01	GND	
	P5	00	GND	

CONN 1

SHEET LOCATION	ROW 1	TERM. NO.	ROW 2	SHEET LOCATION
	P5	41	GND	
	GND	40	GND	
	GND	01	GND	
	P5	00	GND	

CONN 0

NOTES
1. UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE 1/4 W, ±5%.

BRUNING 44231 16042

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS

PRE PRODUCTION APPROVAL | DEV | PROD

ADDED NOTE 1 & REVISED SHEETS 5 & 6.
KL | 3021-02 | | 5-1-73 | R01

REVISED SHEETS 4, 5 & 6.
KL JY | 3021-004 | | 6-6-73 | R02

RELEASED FOR PRODUCTION
MFG. ENG. J. Y. DATE 8/8/73

REVISED SHT'S 4 & 5
BG | 1963 | | 11-9-73 | R03

REVISED SHT'S 2, 3, 5 & 6
35-438 M01 WAS R03.
RP | 2615 | | 10-1-75 | R04

REVISED SHT'S 1 THRU 6.
35-438 M01 WAS R04.
AREA M9: ADDED MANUALS 29-289, 29-486 & 29-487.

WTA | 3613 | M | 10-6-78 | R05

REVISED SHT'S 1 & 5
SHT. 1 AREA S9 35-438 M01 WAS R08

BP | 3886 | R | 5-16-79 | R06

USED IN MANUALS
29-289, 29-486 & 29-487

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL

DISK CONTROLLER	35-428 M01 R09

NOTE
THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

SHEET INDEX	REV. LEVEL	R06	R02	R02	R04	R06	R04
	SHEET NO.	1	2	3	4	5	6

NAME	TITLE	DATE
K. LAFFERTY	DRAFT	10-10-72
H. MATTER	CHK	3-29-73
J. YANG	ENGR	3-29-73
N. MASSI	TEST	7-2-73
J. FISARCIK	DIR ENG	7-2-73

TITLE FUNCTIONAL SCHEMATIC
DISK CONTROLLER

DASH NO. 03021
DRAWING NO. 02-263 R06 D08
SHEET 1 OF 6

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS			
ARGARS GATES A112 & A103 AND RELATED CIR-CUITRY WERE NOT SPECIFD.			
A	[illegible] 26 15		10-1-75 ROI
AREA G2-N2: A32 & A61 WAS SPEC'D AS 19-036 HPO. AREA E7: CAP. 'C2' 470PF WAS CONN. TO A21-08; AREA E8: A9-10 WAS CONN TO A9-09. AREA G7; A18 19-024 WAS NOT SPEC'D. AREA A8: MNEMONIC CEXAMO. SHT LOC 3C1 WAS 3E1. A29-13 WAS CONN TO A18-01			
WTA	97	3613	M 9-28-78 ROZ

P5 —|(— GND
15MF, 20V TANTULUM
C17-C25

P5 —|(— GND
1000PF, 50V
C26-C122

DECOUPLING CAPACITORS

NOTES 1. NORMALLY STRAPPED FOR X'BG', X'CG', X'DG', X'EG', X'FG'.
2. STRAPPED FOR 2200 BPI DISC.

NAME	TITLE	DATE
K. LAFFERTY	DRAFT	9-28-72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
DISK CONTROLLER

TASK NO. 03021
DWG NO. 02-263 R02 D08
SHEET OF 2-

BRUNING 44-231 16042

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS			
AREA A1, CORR. ENG. WAS NOT SPECID.			
W	RP-2423	10-9-77	RO1
AREA E2, F2, G2 & G4: ADDED A170, A172, A169, R84-R88 & C124. REMOVED A2 & C4. SEE RO1 MICROFILM FOR PREVIOUS CONFIGURATION.			
W	3613	M	10-6-78	RO2

BRUNING 44-231 16042

NOTES

NAME: P EDWARDS | DATE: 4-29-77

TITLE: FUNCTIONAL SCHEMATIC
DISK CONTROLLER

DWG NO. 03021
REV 02-263 R02 D08
SHEET OF 3

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
ADDED A175 GATES AREAS L2 & N2.				
KL	JT	3021-004	6-6-73	R02
LOC AB WBTCG1 WAS SECLRO, LOC CB DASH WAS NOT SPECIFIED OVER LSTBY1				
BC	MA	1963	4-4-73	R03
AREA J9: REMOVED SHT. LOC. 5J9 FROM MNEMONIC RDCLK1,				
WA	JW	3613	9-28-78	R04

NOTES

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NAME	TITLE	DATE
P. EDWARDS	DRAFT	2-14-73
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
DISK CONTROLLER

TASK NO. 03021
DWG NO. 02-263 R04 D08
SHEET OF 4

BRUNING 44-231 16042

PERKIN-ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
IN AREA G-6, CM WAS .0022 uF, R65 WAS 47.5K ±0.1 USEC WAS 30 ±3 MSEC.				
KL	JY	3021-02	JS	5-1-73	R01
AREA H9, DELETED INDTA1A, ADDED 6J6				
KL	JY	3021-004	WH	6-6-73	R02

INDXOA
D5 D6
J9 P3.5
C10 2.2 UF 23-001
R53 100Ω
R58 15K
R59 10K
C11 .001UF DA 23-001
A56 19-092 DUAL ONE SHOT (5 ±1 u SEC)
R60 1K
R48 100Ω
R49 100Ω
R50 100Ω
R52 100Ω
R51 100Ω
R54 100Ω
R55 100Ω
R56 100Ω
A55 19-015 HG
A72 19-015 HG
A82 19-021 P
A93 19-021 P
A62 19-021 P
A83 19-095
A84 19-095
A94 19-089
A68 19-095
A95 19-031 ONE SHOT (95 ±4 u SEC)
A97 19-031 ONE SHOT (36 ±4 u SEC)
A66 19-028 4 BIT BINARY FULL ADDER
A114 19-028 4 BIT BINARY FULL ADDER
A107 19-092 DUAL ONE SHOT (6 ±1 USEC)
A107 19-092 DUAL ONE SHOT (150 NSEC)
A76 19-016 HG
A86 19-024 HA
A87 19-029 XOR
A98 19-009 G
A116 19-015 HG
A117 19-024 HA
A118 19-016 HG
A96 19-016 HG
A106 19-024 HA
A115 19-029 XOR
A93 19-021 P
A117 19-024 HA
A82 19-021 P
A69 19-009 G
A64 19-009 G
A108 19-003 G
A126 19-089
A127 19-095
A128 19-095
A129 19-024 HA
A125 19-016 HG
A73 19-015 HG
A74 19-016 HG
A75 19-024 HA
A85 19-017 HG
A105 19-016 HG
A106 19-024 HA
A62 19-021 P
A169 19-015 HG

R61 10K, R62 2.2K, C12 .022 UF
R63 10K, R64 1K, C13 .022 UF
R65 20K, R66 10K, C14 .001 UF, D7 23-001
R67 1K, R68 1K, R69 1K
R71 2.2K, R72 1K, R73 1K, R74 22 K
R70 1K, R89 SEE NOTE 1
R47 100Ω, R57 100Ω

INDXO 114-3
SMO 113-3
SEC10 211-3
SEC20 111-3
SEC40 112-3
SEC80 110-3
SEC160 109-3
SEC320 210-3
TAENI 3G3
DIR071 6N8
DIR061 6N8
DIR051 6N8
DIR041 6N8
DIR031 6L9
DIR021 6L9
DIR011 6L9
DIR001 6L9
CY2561 6L9
SEC161 C4
SEC81 C3
SEC41 C3
SEC21 C3
SEC11 C2
TA10 103-3
TA20 204-3
TA40 104-3
TA80 203-3,
TA160 102-3
TA320 101-3
TA640 106-3
TA1280 105-3
TA2560 205-3
HIDEN 201-3
CNTCMO 2S8
GCLRO 2S6
OVERRUNO 6D3
CMPCLO J8 4R7
CBSYO 3D3
CBSY1 2A8
STCLRO 4H9
CNTCM1 4A5
IDXST1 4J8
SM1 4J4
FRSRW1 3H7
PSF E7
PREAM E9
SECLRO
WTSTO H8
WTSTO K2, F4
WTGT1 3D1
WBTCG1 3C2 4A8
WTCLK1
WGBT71 4A9
WTOSC1 2K8
ENSYN1 S3 4K2 4J2 6F9
CYOUT1
WLSBY1 S1, 4C7
WTEDO 4D8
ENDTA0 S2
DOROT1 6R7
BYENDI S2
PSH N7, 6F4
ERDI 4E6
RDFOT1 4F5
WT1 4F6
CONTO 4H8
WLDOR S4
WTFOT1 4F5
DREAM J3
SCCMPO 6B6
SCCMPI 4A3
RDCLKO 108-3
RDCLK/A 6A9
RDTA0 115-3
HIDEN1 6A5
NTRQC1 6K1
INAKCO 2N4
OPCMPO 4N7
WLSBY1 H5
ENDTA0 H6 6B7
BYENDC 4C9
BYENDI H6, 4J3
ENSYN1 J4
WCBCTO 4G5
WLDOR E8 6L5
WTDA0 107-3
WCYCK 6B8
ARDGTO 6B6
DRDGTO M7
BIT71 4R2
RDGT1 3B1
RLDDO1 6J5
WT DTA0 6B7
CKCY1 6A9
RDENDO 4J7
CKCY0 4C9
RDTAC0 6B8
DRBCG1 4J9
DRBCG0 6F6
SHDIR0 6B8
DRDGTO M5 6L7
DRDGT1 6A7
SYND1 6C6
CKCY20 4C7
RDTA0
INDTA1 4L8, 6J6
SMCLRO H8

NOTES
1. AG8-07 ISOLATED TO FACILITATE AUTOMATIC TESTING

REVISIONS				
SECLRO WAS SPECIFIED AS GOING TO 4A8				
BG	BEK	1963	WH	10-29-73	R03
AREA E1, R58 WAS 10 K. AREA G6, R65 WAS 15K.				
BP	WH	2615	—	10-1-75	R04
AREA A4: MNEMONIC TAENI & SHT. LOC. 3G3 WAS NOT SPEC'D; AREA M2: MNEM. WBTCG1 SHT LOC. 3C2 WAS 3E2, AREA J9: RDCLK1A, 6A9 WAS SPEC'D AS RDCLK1, 4J9.				
BP	WH	3613	M	9-28-78	R05
AG8-07 WAS CONN. TO AG8-09 ADDED R89 TO AG8-07. ADDED NOTE 1.				
BP	WH	3886	R	1-5-79	R06

NAME	TITLE	DATE
G. JENSEN	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
DISK CONTROLLER

TASK NO 03021
DWG NO 02-263 R06 D08
SHEET OF 5 -

BRUNING 44-231 16042

PERKIN ELMER
Computer Systems Division
Oceanport, N.J. 07757

REVISIONS				
IN AREA E-6, ADDED C123.				
KL	J.S	3021-02	5-1-73	R01
IN AREA J-6, INDTAI WAS INDTAIA, 5S9 WAS 5R9; AREA E-6, 4R2 WAS 4L2 AREA M5'S ADDED 19-045 & 19-016, AREA A8 ADDED 19-017, AREA B9 19-016 WAS 19-024				
BG	JS	3021-004	6/26/73	R02
AREA N6, R78 WAS 330 OHMS 1/2W.				
JS	DC	2613	10-1-75	R03
AREA B9: PINS 03, 04 & 05 OF A140 (19-024) WERE CONN. TO PIN 02 OF A13 (19-016). MNEMONIC RDCLKIA WAS NOT SPEC'D.				
WA	GJ	3613	9-28-78	R04

NOTES

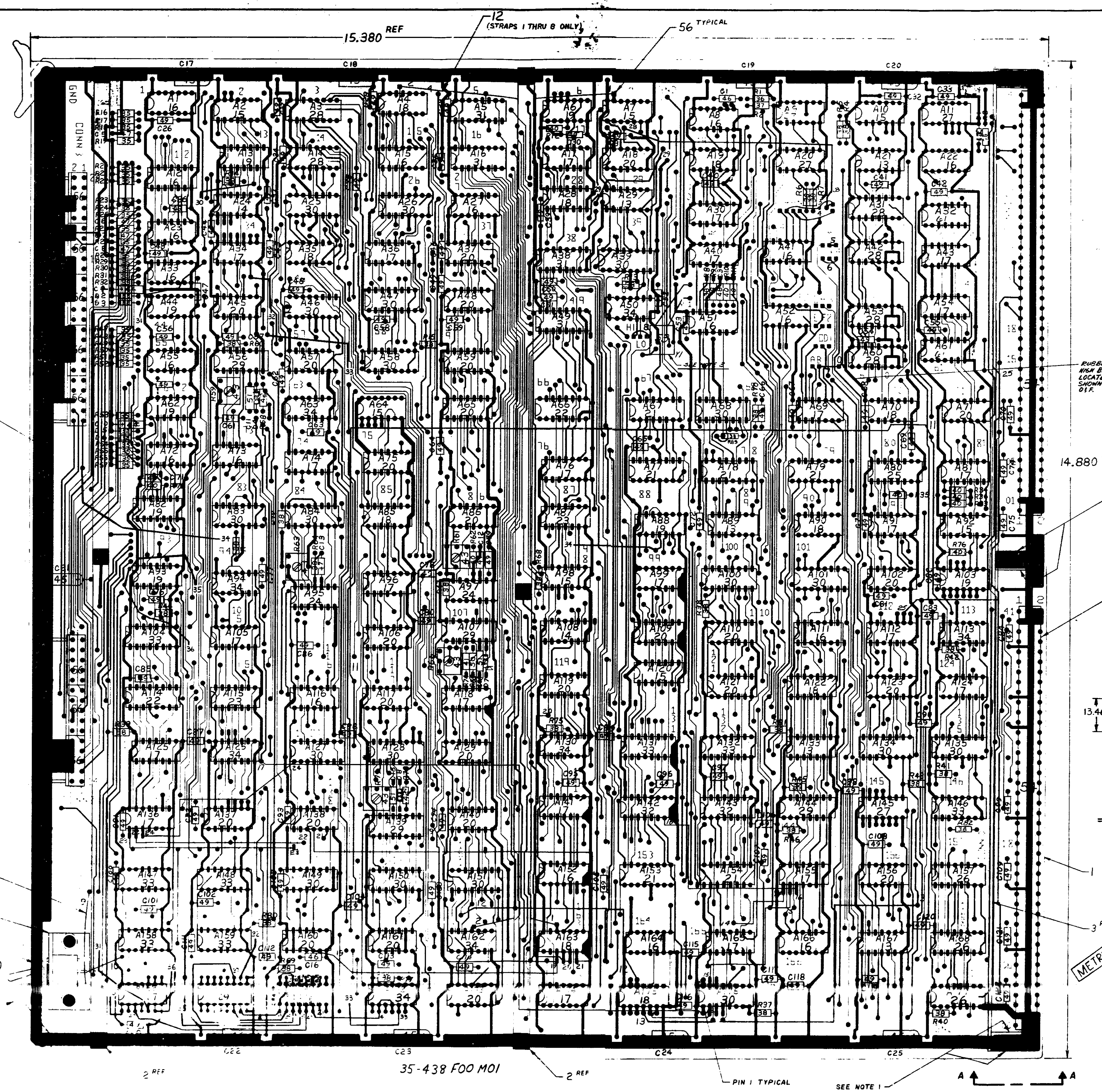
NAME	TITLE	DATE
K. LAFFERTY	DRAFT	2-26-73
	CHK	
	ENGR	
	DIR ENG	

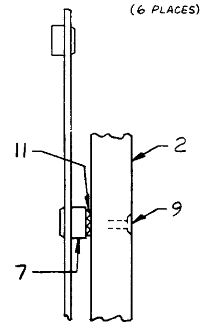
TITLE FUNCTIONAL SCHEMATIC
DISK CONTROLLER

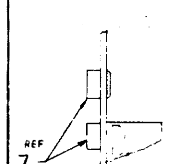
TASK NO 03021
DWG NO 02-263R04D08
SHEET 6 OF 6

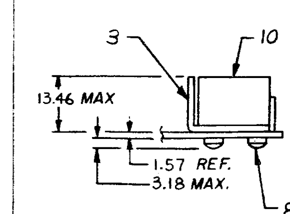
GRUNING 44-231 16042

MILLIMETER	INCH
1.57	.062
3.18	.125
13.46	.530









PARTIAL VIEW A-A

REVISIONS

UNDER A107 - CHANGED SIZE OF R65 & C14 WAS SPECIFIED AS ITEM 50, ADDED C123.

KL		3021-02		5-1-73	R01

ADDED STRAPS 11 THRU 24; ON ITEM 57 MOVED LOCKWASHER TO [illegible] SIDE OF SWITCH.

BG		3021-504		6-8-73	R02

RELEASED FOR PRODUCTION — MFG ENG. DATE

REVISED TO REFLECT NEW COPPER

BG		1963		[illegible]	R03

STRAP 15 WAS WIRED TO A176-14.

GJH		2004		1-2-74	R04

MOVED CRYSTAL TO RELIEVE STRESS ON LEADS. CHANGED NOTE 3.

GJH		2025		1-2-74	R05

ADDED R82 & R83

BG		2203	—	[illegible]	R06

STRAP 25 WAS NOT SPEC'D. REVISED TO REFLECT NEW COPPER AREA [illegible] WAS SPEC'D AS ITEM 39 AREA A107, R65 WAS SPEC'D AS ITEM 42, & AREA A139, R78 WAS SPEC'D AS ITEM 39

		2615	—	10-7-75	R07

SHT 2 & VARIATION BLOCK WERE NOT SPEC'D

		2636	—	10-[illegible]-75	R08

SHT 2, AREA A94: CUT UNDERNEATH A94 WAS SHOWN INCORRECTLY

		2831	—	10-8-76	R09

SHT 1 & 2 REMOVED C2 ITEM 55 & REVISED TO REFLECT NEW (R06) COPPER, SHT 1 - ADDED STRAP #26 & 27 SHT 2 ADDED STRAP #30 & 31 SHT 1 & 2 - IC A32 WAS ITEM 27 AND IC A61 WAS ITEM 27.

FM		3443		11-5-77	R10

REVISED CIRCUITRY TO REFLECT NEW COPPER. SHT 1, REMOVED STRAP #26 FROM A8-08 TO A62-13. SHT 2, REMOVED STRAP #30 FROM A8-08 TO A62-13. SHTS. 1 & 2: ADDED I.C A170 AREA A171: ADDED RES. R84 - R88, CAP C124. REMOVE R83 BELOW A68 & A69. SHT. 1, ADDED STRAPS 28 - 41. SHT 2, ADDED STRAPS 32-45. ADDED METRIC DIM. & TABLE. REMOVED STRAP #27 FROM A8-09. SHT. 2 REMOVED STRAP #31 FROM A8-09.

		3613	M	10-4-78	R11

ADDED RESISTOR R89 TO A68

BFP		3886	R	5-4-79	R12

PART NO	VARIATION	
35-438M01	F00	PER SHT 1
35-438M01	F01	PER SHT 2

METRIC

SCALE 2:1

COMPONENT	REF DESIGNATION
STRAPS	1-25, 28-41
CRYSTAL	Y1
RESISTOR	R1-R82, R84-R89
DIODE	D1-D82,
CAPACITOR	C1, C3, C5-C124
INT CIRCUIT	A1-A170, A172-A177

	TITLE	DATE
F. LAFFERTY	DRAFT	3-7-73
H. MATTER	CHK	3-29-73
J. YANG	ENG	3-29-73
H. ROSS	Q.C.	7-2-73
J. PISARCIK	MGR	7-2-73

ASSEMBLY
CARTRIDGE DISK CONTROLLER

TASK NO. 03021
DWG NO. 35-438M01R12 E03
SHEET 1-2

MILLIMETER	INCH
1.57	.062
3.18	.125
13.46	.530

REVISIONS

15.380 REF

12 (STRAPS 1 THRU 8 ONLY)

56 TYPICAL

14.880 REF

7 MOUNT ON SOLDER SIDE AFTER FLOW SOLDER (6 PLACES)

3 CUTS APP SIDE

58 (STRAPS 9-29 & 32-45)

4,8,11

57 (NOW SUPPLIED WITH SWITCH)

5,6

2 REF

PIN 1 TYPICAL

SEE NOTE 1

SEE NOTE 2

RUBBER STAMP 1/8" HGT BLK LETTERING LOCATE APPROX AS SHOWN FOR SIZES 01A

3 REF

1

3 REF

13.46 MAX

1.57 REF.

3.18 MAX.

PARTIAL VIEW A-A

METRIC

SCALE 2:1

COMPONENT	REF DESIGNATION
STRAPS	1-29, 32-45
CRYSTAL	Y1
RESISTOR	R1-R82, R24-R89
DIODE	D1-D82,
CAPACITOR	C1, C3, C5-C124
INT CIRCUIT	A1-A170, A172-A177

35-438 F01 M01

NOTES:
1. HEADER STIFFENER (ITEM 3) TO BE SOLDERED TO GND BUS AT 2 END POINTS & CENTER POINT.
2. CONTACTS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.
3. CRYSTAL (ITEM 53) MUST BE SECURED TO BOARD WITH THERMOFORCED TAPE. THE LEADS MUST BE SLEEVED.

	TITLE	DATE
K. LAFFERTY	DRAFT	3-27-73
H. MATTEN	CHK	3-29-73
J. YANG	ENG	3-11-73
M. ROSS	QC	7-2-73
	MFG	7-2-73

ASSEMBLY CARTRIDGE DISK CONTROLLER

TASK NO. 05021 DWG NO. 35-438M01-A1 EC0 2-2

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